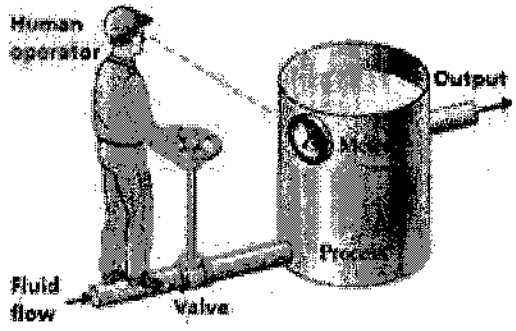
The maximum mark for the examination paper is 90 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

- Clarify your answer with the suitable sketches as you can.
- Please use a pen or heavy pencil to ensure legibility.
- Please attempt all questions.



QUESTION NUMBER ONE [40 MARKS]

1. Modify the block diagram to show how the fluid level of the system used a human operator as part of a control system could be digitally controlled. Afterward, explain the reasons for the popularity of digital control systems. [8 Marks]

2. A S/H will be used with a 12-bit, unipolar ADC with a 30μs conversion time. The S/H switch ON resistor is 10Ω, and its OFF resistance is 10MΩ. The voltage follower input resistance is also 10MΩ while the signal source output resistance is 50Ω.
   a) What value of capacitor should be used? [4 Marks]
   b) Determine the sampling cutoff frequency. [2 Marks]
   c) What is the digital word that results from a 3.127 analogue signal input to a 5-bit ADC with a 5V reference? [4 Marks]

3. The specification for an antenna analog tracker are:
   1. Overshoot to step input less than 16%.
   2. Settling time to be less than 10 seconds.
   3. Sampling time to give at least 10 samples in a rise time.

   Hint: $t_r = \frac{\pi - \theta}{\omega_d}, \theta = \tan^{-1}\sqrt{\frac{1-\xi^2}{\xi}}$

   Draw the corresponding regions in the z-plane. [8 Marks]

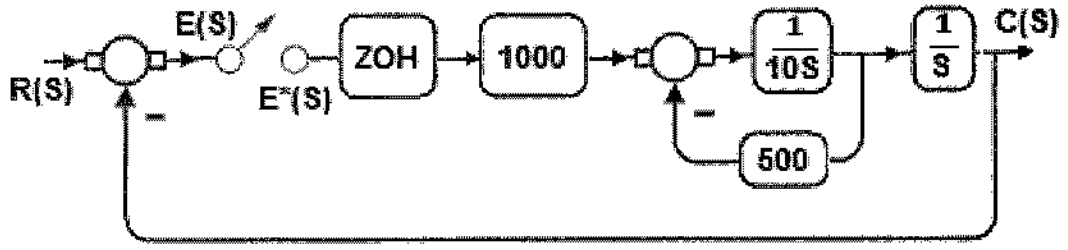
4. Derive the discrete-time transfer function of the following continuous-time plant (Hint: Use a zero-order hold element and assume the sampling time T=0.2 sec):

$$P(S) = \frac{1}{S^2 + 3S + 2}$$

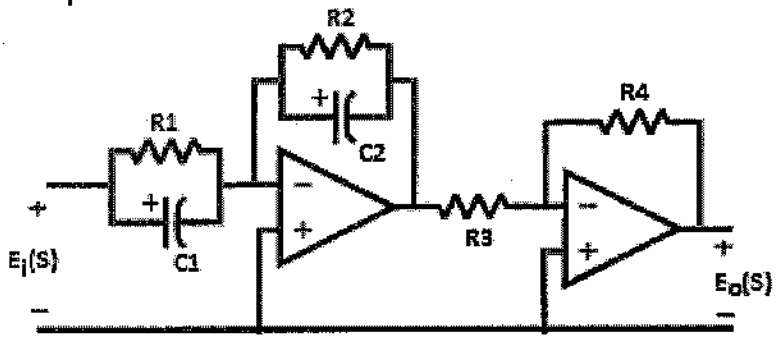
   Henceforth, suppose that a factor K is added to the plant, using Jury stability test find out the range of K for which the system is stable. [14 Marks]

QUESTION NUMBER TWO [50 MARKS]

1. Calculate the steady state errors for unit step, unit ramp and unit parabolic inputs for the system shown in the following figure. Let T = 0.1 second. [10 Marks]



2. Shows that the transfer function for the following active network architecture has the phase lead / lag characteristics. Then, tell me why lead compensation may degrade steady state error performance? [10 Marks]

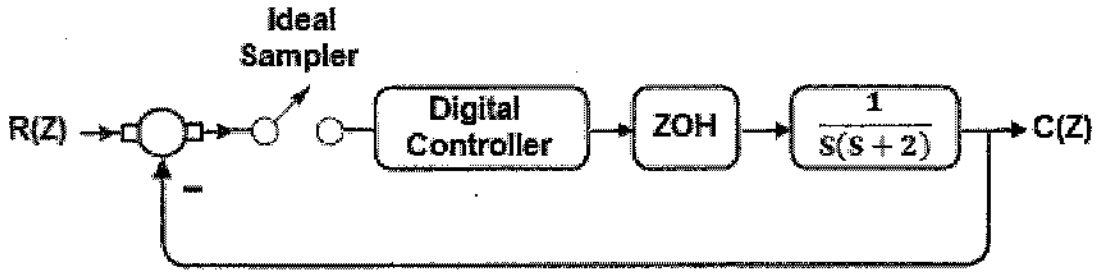


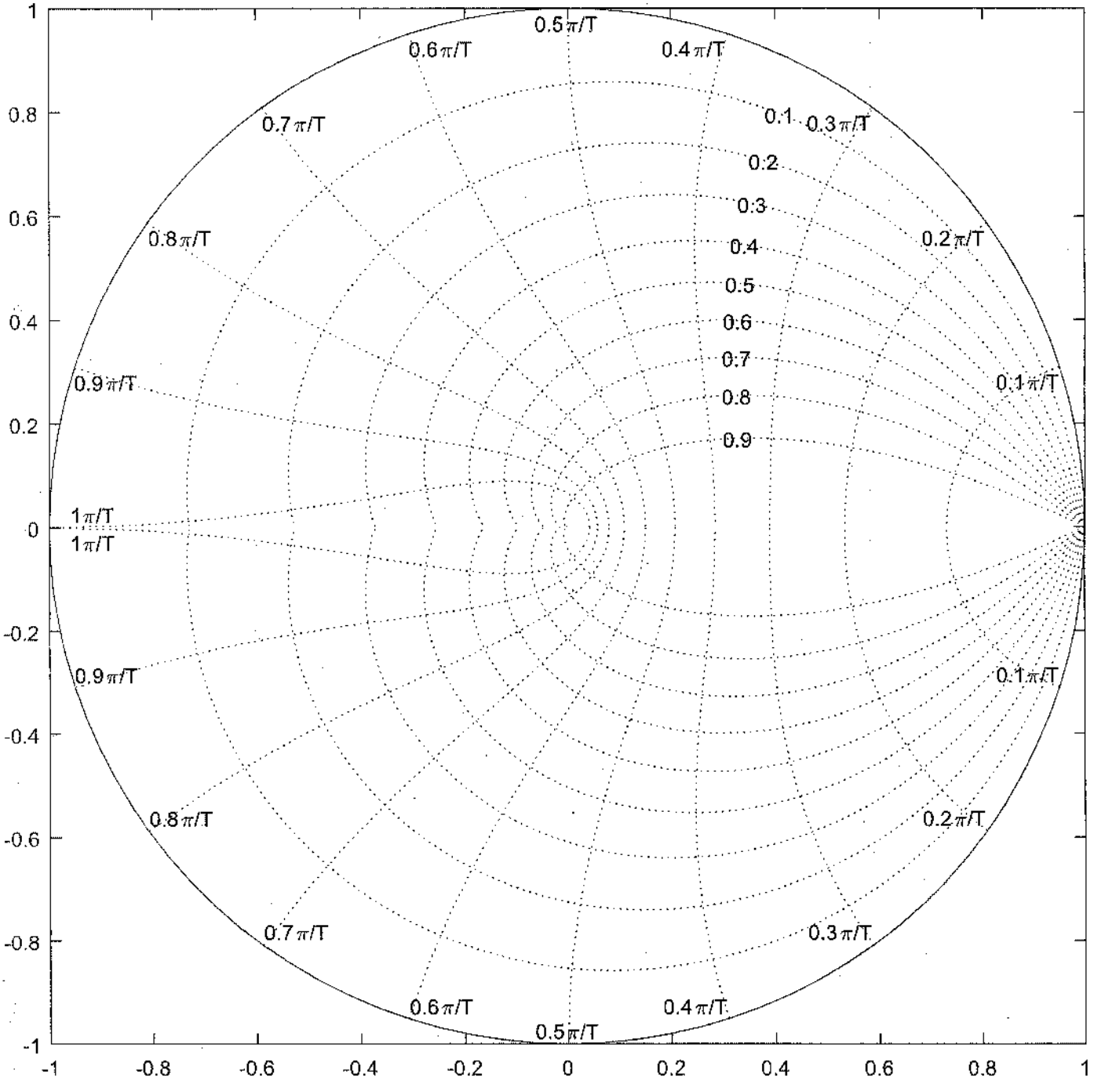
3. Given is a plant described by the following transfer function:

$$G_P(S) = \frac{1}{S(S+1)}$$

Construct the approximate equivalent discrete time controller by the method of backward rectangular integration such that step response of the closed loop shows the following properties: maximum overshoot is 0.16 and settling time is 2 second. Choose sampling period = 0.1 second. [15 Marks]

4. Consider the digital control system shown in figure. In the z-plane, design a digital controller such that the dominant closed loop poles have a damping ratio ξ of 0.5 and a settling time of 2 sec. The sampling period is assumed to be 0.2 sec. [15 Marks]




0.5π/T
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1