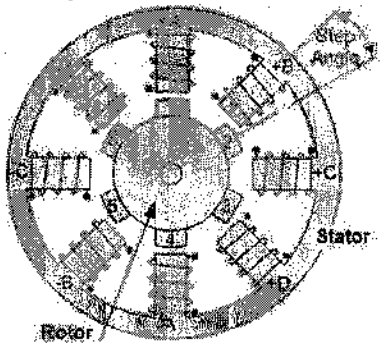
KAFR-ELSHIEKH UNIVERSITY
FACULTY OF ENGINEERING
TIME ALLOWED: 3 HOURS

ELECTRICAL ENGINEERING DEPARTMENT
COMPUTER ENGINEERING AND SYSTEMS BRANCH
2ND YEAR FINAL EXAM OF 2ND SEMESTER 2018 - 2019
MICROPROCESSOR SYSTEMS [CODE NO. ECS 2006]

The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

- Clarify your answer with the suitable sketches as you can.
- Please use a pen or heavy pencil to ensure legibility.
- Please attempt all questions.



QUESTION NUMBER ONE [20 MARKS]

1. Differentiate between isolated and memory mapped I/O scheme. Then, explain the term handshaking as it applies to microprocessor I/O systems (Hint: I expect to see a timing diagram that illustrates the term handshaking). [6 Marks]
2. How is 82C55 (Programmable Peripheral Interface) configured if its control register contains 9Bh. Henceforth, design a stepper motor controller and write an assembly program to rotate the shaft of 4 phase stepper motor in clockwise 5 rotations and in anticlockwise 5 rotations. The base address is 00H. [7 Marks]
3. With neat diagram indicate how keyboard is interfaced to 8088 μp through 82C55. Henceforward, write the lines' code required to place logic 1 on the PC7 pin of the 82C55 during strobed input operation. [7 Marks]

QUESTION NUMBER TWO [25 MARKS]

1. Many EPROM available today have an access time of a 450 ns, which is to slow for the 5MHz 8088 μp. Explain how we can avoid this problem. After that, with neat diagram indicate how an 8088 microprocessor connected to three 27256 memory devices in the address range that begins at location E8000H and continues through location FFFFFH. [8 Marks]
2. Design an address decoding logic using eight 64K x 8 SRAM memory devices, a PLD, and an OR gate to interface a total of 512 KB memory system with 80486 μp in the address range that begins at location 02000000H through 0203FFFFH. [9 Marks]
3. Describe software interrupts available in INTEL family. How interrupts are executed in real mode. Then, design a circuit to implement a hardware interrupt for interrupt vector type 41H (including INTR, $\overline{\text{INTA}}$, and a buffer 74LS244 to pass 41H to data lines). [8 Marks]

QUESTION NUMBER THREE [15 MARKS]

1. Assume that the first six memory-reference instructions in the basic computer are to be changed to the instructions specified in the following table. EA is the effective address that resides in AR during time T4. Assume that the adder and logic circuit perform the exclusive-OR operation AC←AC ⊕ DR. Assume further that the adder and logic circuit cannot perform subtraction directly. The subtraction must be done using the 2's complement of the subtrahend by complementing and incrementing AC. Give the sequence of register transfer statements needed to execute each of the listed instructions starting from timing T4. Note that the value in AC should not change unless the instruction specifies a change in its content. You can use TR to store the content of AC temporary or you can exchange DR and AC. [5 Marks]

Symbol	Opcode	Symbolic designation	Description in words
XOR	000	$AC \leftarrow AC \oplus M[EA]$	Exclusive-OR to AC
ADM	001	$M[EA] \leftarrow M[EA] + AC$	Add AC to memory
SUB	010	$AC \leftarrow AC - M[EA]$	Subtract memory from AC
XCH	011	$AC \leftarrow M[EA]$, $M[EA] \leftarrow AC$	Exchange AC and memory
SEQ	100	If $(M[EA] = AC)$ then $(PC \leftarrow PC + 1)$	Skip on equal
BPA	101	If $(AC > 0)$ then $(PC \leftarrow EA)$	Branch if AC positive and non-zero

2. The operations to be performed with a flip-flop F (not used in the basic computer) are specified by the following register transfer statements:

xT_3: $F \leftarrow 1$ Set F to 1
yT_1: $F \leftarrow 0$ Clear F to 0
zT_2: $F \leftarrow \overline{F}$ Complement F
wT_5: $F \leftarrow G$ Transfer value of G to F

Otherwise, the content of F must not change. Draw the logic diagram showing the connections of the gates that form the control functions and the inputs of flip-flop F. Use a JK flip-flop and minimize the number of gates. [5 Marks]

3. Show the complete logic of the interrupt flip-flops R in the basic computer. Use a JK flip-flop and minimize the number of gates. [5 Marks]

Fetch	$R'T_0$:	$AR \leftarrow PC$
	$R'T_1$:	$IR \leftarrow M[AR]$, $PC \leftarrow PC + 1$
Decode	$R'T_2$:	$D_0, \ldots, D_7 \leftarrow$ Decode $IR(12\text{–}14)$, $AR \leftarrow IR(0\text{–}11)$, $I \leftarrow IR(15)$
Indirect	D_7IT_3:	$AR \leftarrow M[AR]$
Interrupt:		
	$T_0T_1T_2(IEN)(FGI + FGO)$:	$R \leftarrow 1$
	RT_0:	$AR \leftarrow 0$, $TR \leftarrow PC$
	RT_1:	$M[AR] \leftarrow TR$, $PC \leftarrow 0$
	RT_2:	$PC \leftarrow PC + 1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$
Memory-reference:		
AND	D_0T_4:	$DR \leftarrow M[AR]$
	D_0T_5:	$AC \leftarrow AC \wedge DR$, $SC \leftarrow 0$
ADD	D_1T_4:	$DR \leftarrow M[AR]$
	D_1T_5:	$AC \leftarrow AC + DR$, $E \leftarrow C_{out}$, $SC \leftarrow 0$
LDA	D_2T_4:	$DR \leftarrow M[AR]$
	D_2T_5:	$AC \leftarrow DR$, $SC \leftarrow 0$
STA	D_3T_4:	$M[AR] \leftarrow AC$, $SC \leftarrow 0$
BUN	D_4T_4:	$PC \leftarrow AR$, $SC \leftarrow 0$
BSA	D_5T_4:	$M[AR] \leftarrow PC$, $AR \leftarrow AR + 1$
	D_5T_5:	$PC \leftarrow AR$, $SC \leftarrow 0$
ISZ	D_6T_4:	$DR \leftarrow M[AR]$
	D_6T_5:	$DR \leftarrow DR + 1$
	D_6T_6:	$M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$
Register-reference:		
		$D_7I'T_3 = r$ (common to all register-reference instructions)
		$IR(i) = B_i$ $(i = 0, 1, 2, \ldots, 11)$
	r:	$SC \leftarrow 0$
CLA	rB_{11}:	$AC \leftarrow 0$
CLE	rB_{10}:	$E \leftarrow 0$
CMA	rB_9:	$AC \leftarrow \overline{AC}$
CME	rB_8:	$E \leftarrow \overline{E}$
CIR	rB_7:	$AC \leftarrow$ shr AC, $AC(15) \leftarrow E$, $E \leftarrow AC(0)$
CIL	rB_6:	$AC \leftarrow$ shl AC, $AC(0) \leftarrow E$, $E \leftarrow AC(15)$
INC	rB_5:	$AC \leftarrow AC + 1$
SPA	rB_4:	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$
SNA	rB_3:	If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$
SZA	rB_2:	If $(AC = 0)$ then $PC \leftarrow PC + 1$
SZE	rB_1:	If $(E = 0)$ then $(PC \leftarrow PC + 1)$
HLT	rB_0:	$S \leftarrow 0$
Input-output:		
		$D_7IT_3 = p$ (common to all input–output instructions)
		$IR(i) = B_i$ $(i = 6, 7, 8, 9, 10, 11)$
	p:	$SC \leftarrow 0$
INP	pB_{11}:	$AC(0\text{–}7) \leftarrow INPR$, $FGI \leftarrow 0$
OUT	pB_{10}:	$OUTR \leftarrow AC(0\text{–}7)$, $FGO \leftarrow 0$
SKI	pB_9:	If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$
SKO	pB_8:	If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$
ION	pB_7:	$IEN \leftarrow 1$
IOF	pB_6:	$IEN \leftarrow 0$