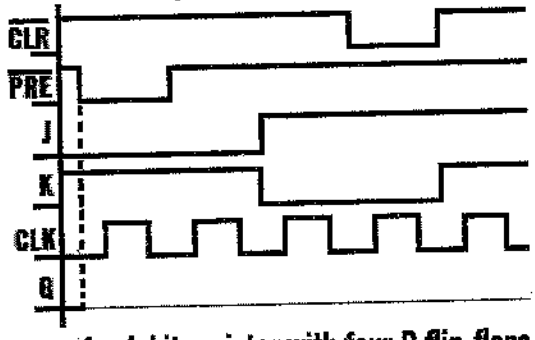
The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

QUESTION NUMBER ONE [25 MARKS]

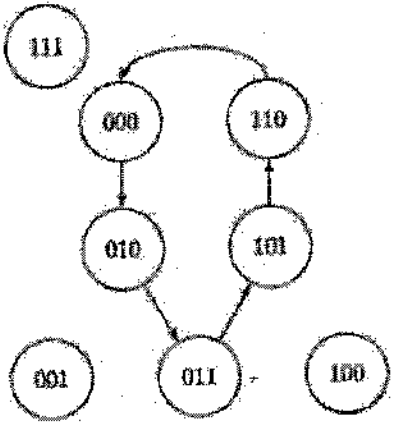
1. What is the essential difference between latch and flip flop? After that, complete the given timing diagram for a JK flip flop with a falling-edge trigger and asynchronous active-low clear and active-low preset inputs. [5 Marks]



2. Draw the logic diagram of a 4-bit register with four D flip-flops and four 4X1 multiplexers with mode selection S0 and S1. The register operates according to the following table: [5 Marks]

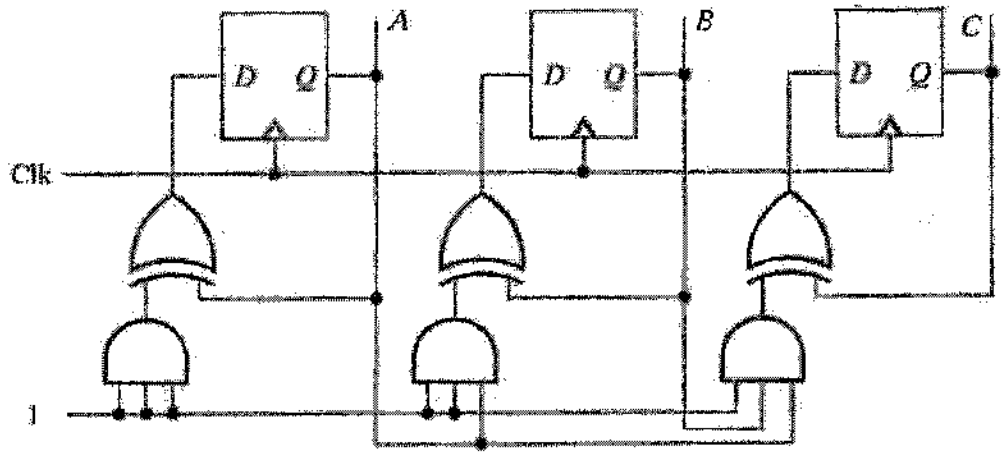
S0	S1	Register operation
0	0	No change
0	1	Complement the four outputs
1	0	Clear register to 0
1	1	Load parallel data

3. Any flip-flop can be implemented from another type with suitable logic applied to the latter's inputs. Show how to implement a J-K flip flop starting with an X-Y flip flop. The X-Y flip-flop has four operations, clear to 0, complement, no change, and set to 1, when inputs X and Y are 00, 01, 10, and 11, respectively. [5 Marks]
4. Design a sequential circuit that meets the following state diagram. The final circuit must be analyzed to ensure that it is self-correcting. [10 Marks]



Question Number Two [35 Marks]

1. For the following clocked sequential circuit:
   a) Drive a state table and draw a state diagram for the circuit.
   b) Redesign this circuit by replacing the D flip-flop with a JK flip-flop. [15 Marks]



2. How many 32 K x 8 RAM chips are needed to provide a memory of 128 K-bytes? How many lines of the address must be used to access 128 K-bytes? How many of these lines are connected to the address inputs of all chips? How many lines must be decoded for the chip-select inputs? Show the external connections that illustrate the interconnection of the necessary number of 32K x 8 RAM chips to form a 128 K x 8 bit RAM. [5 Marks]

3. With neat diagram indicate how DRAM is different from SRAM? Then, write a brief note on the various types of ROM devices that you are familiar with. [10 Marks]

4. Design a 1-bit of the universal shift register to the following specifications. The internal storage element will be positive edge-triggered D flip-flop. Besides the clock, the shifter stage has two external control inputs S_0 and S_1 and thee data inputs S_R, S_L and S_{PL}. S_R is the data being shifted from right, S_L is the data being shifted from left, and S_{PL} is the parallel-load data. The current value of the flip-flop will be replaced according to the following setting of the control signals: S0=S1=0: replace D with S_{PL}; S0=0, S1=1: replace D with S_L; S0=1, S1=0: replace D with S_R; S0=S1=1: hold the current state of the universal shift register. [5 Marks]