KAFR-ELSHIEKH UNIVERSITY
FACULTY OF ENGINEERING
TIME ALLOWED: 3 HOURS

ELECTRICAL ENGINEERING DEPARTMENT
COMPUTER ENGINEERING AND SYSTEMS BRANCH
1ST YEAR FINAL EXAM OF 1ST SEMESTER 2020 - 2021
LOGIC CIRCUITS [CODE NO. ECS 1004]

The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

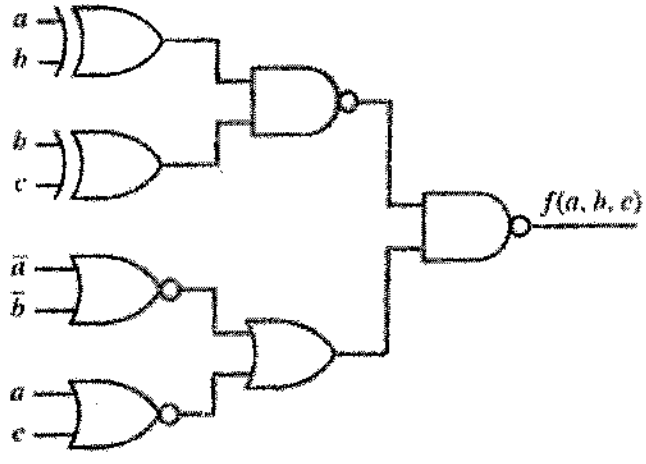
- Clarify your answer with the suitable sketches as you can.
- Please use a pen or heavy pencil to ensure legibility.
- Please attempt all questions.

QUESTION NUMBER ONE [25 MARKS]

1. What is the range of numbers which can be represented by 7 bits if we are representing two's complement integers (express as the formula and as decimal numbers)? Assume 7 bit numbers, find (B-A) for A=22 and B=53 in three different forms. [6 Marks]

2. A and B are two 8-bit, signed binary integers. B is given as B = 10011101. If we perform the operation A-B using the 2's complement system, overflow occurs and the most significant bit of the 8-bit result 1. What is the sign of A (positive or negative)? Why? Write the smallest possible integer A that can constitute this situation (result and overflow). [4 Marks]

3. Reduce the following circuit using theorems and axioms of Boolean algebra to obtain the most compact form. After that, determine the minimum number of NAND gates required to implement the following expression. $F = A + A\overline{B} + A\overline{B}C$ [8 Marks]



X	Y	Z
0	0	Z=A
0	1	Z=B
1	0	Z=A+B
1	1	Z=A-B

4. In digital computer it is necessary to have a combinational circuit that can performs different operations on two 4-bit integers A= A3 A2 A1 A0 and B = B3 B2 B1 B0. The type of these operations is determined by the inputs X and Y as shown in the above table. Design and draw this combinational circuit using one 4-bit full adder, the minimum number of multiplexers, and other necessary logic gates. [7 Marks]

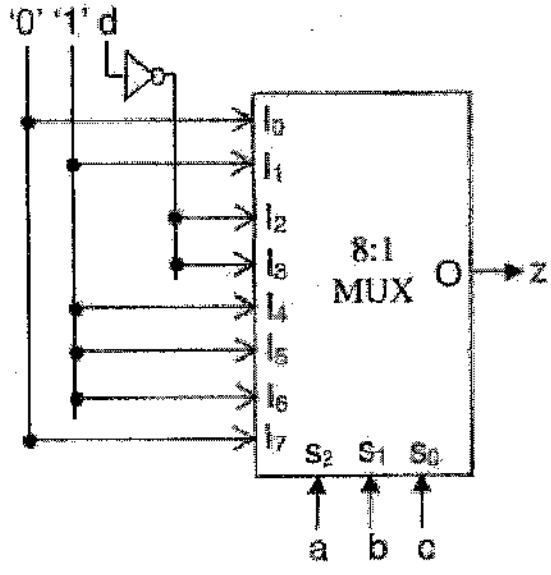
Question number two [35 Marks]

1. Implement the circuit defined by equation F(a, b, c, d) $= \sum(0,5,6,7,11)$ using:
   a) 4-to-1 multiplexers and logic gates.
   b) 2-to-4 decoders with non-inverted outputs and logic gates. [10 Marks]

2. Draw a flow chart that corresponds to the binary division process. After that, show the step by step multiplication process using Booth algorithm when the multiplicand is -6 and the multiplier is 2. [8 Marks]

3. Design a BCD adder/subtractor using the least number of 4-bit binary adder chips and other necessary gates. This circuit should receive two 4-bit numbers A and B and should produce 4-bit sum/difference and a carry/borrow output. [7 Marks]

4. The given combinational circuit has four inputs (a, b, c, d) and one output (Z). Construct the truth table of this circuit and write the expression of the logical function F (a, b, c, d). Then minimize the expression using Karnaugh map. [6 Marks]



5. For the logic circuit shown in the below figure, what is the required input condition (A, B, C) to make the output X is equal 1. [4 Marks]