KAFR-ELSHIEKH UNIVERSITY
FACULTY OF ENGINEERING
TIME ALLOWED: 3 HOURS

ELECTRICAL ENGINEERING DEPARTMENT
COMPUTER ENGINEERING AND SYSTEMS BRANCH
2ND YEAR FINAL EXAM OF 1ST SEMESTER 2020 - 2021
MICROPROCESSOR SYSTEMS [CODE NO. ECS 2006]

The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

- Please use a pen or heavy pencil to ensure legibility.

QUESTION NUMBER ONE [25 MARKS]

1. What are the main differences between the microcontroller and microprocessor? [5 Marks]

2. Answer the following questions: [8 Marks]
   a) Fill in the missing numbers in the following physical address pair: 17?5 : ??B=?2AC?
   b) What is the range of numbers which can be represented by 8 bits if we are representing two's complement integers (express as the formula and as decimal numbers)?
   c) Give the possible values of the 8-bit binary number N which when added to 8-bit number 47H, most significant bit [MSB] equal to "1" and we have no overflow.
   d) What would be the offset address required to point to a destination operand stored at address $002C3_H$ if the contents of the corresponding segment register are $002A_H$?

3. Assume that stack is in the state shown in Fig. [A], and that the instruction POP AX and POP BX are executed in that order. What value would be popped from stack? Into which register would it be popped? What is new address of the top of stack? [5 Marks]

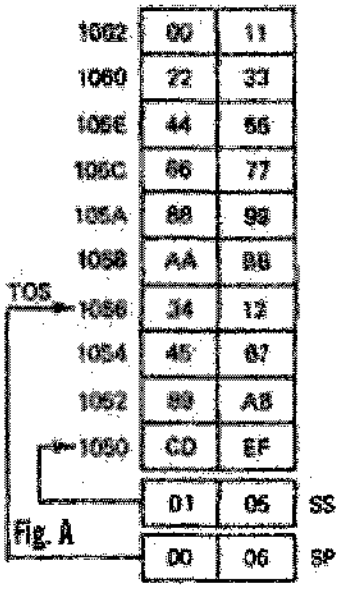


Fig. A

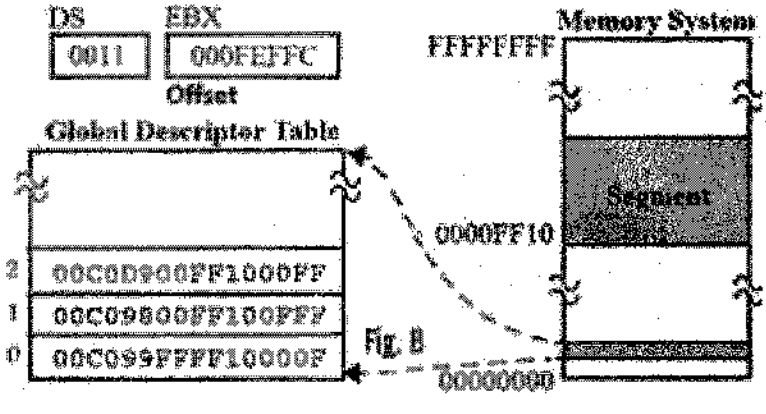


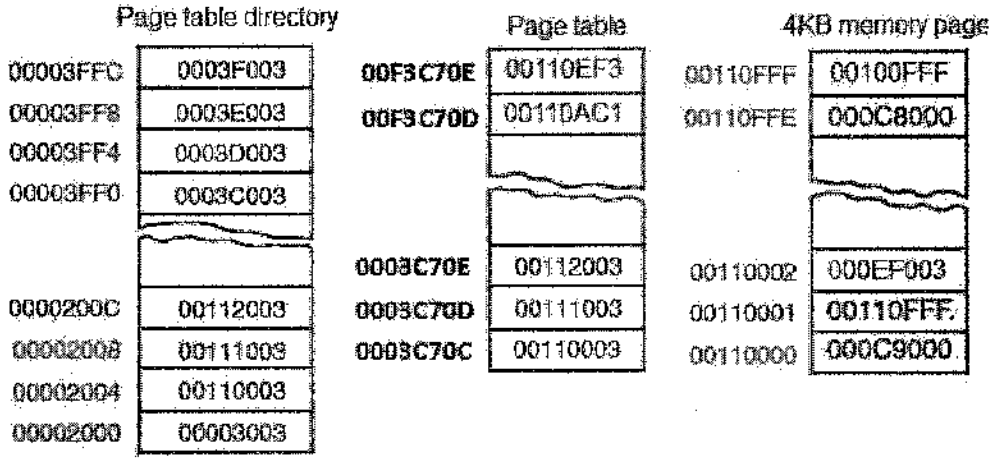
Fig. B

4. For a Core2 descriptor that contains a base of 00280000_H, a limit of 00010_H, and G=1, what starting and ending locations are addressed by this descriptor? After that, use the descriptor definition to decode the appropriate descriptor shown in Fig. [B]. [7 Marks]

Question number two [35 Marks]

1. Answer the following questions: [15 Marks]
   a) The instruction MOV BL, AL stands for move the byte contents from source register AL to destination register BL. Show how to encode the instruction in machine code. The opcode for move operation is 100010.
   b) The instruction ADD AX, [SI] stands for add the 16-bit contents of the memory location indirectly specified by SI to the contents of AX. Encode the instruction in machine code. The opcode for add is 000000.
   c) What is the machine code for the instruction XOR CL, [1234_H]. This instruction says to exclusive-OR the byte of data at memory address 1234_H with the byte contents of CL. The opcode for exclusive-OR is 001100.
   d) The instruction ADD [BX+DI+1234_H], AX means add the word contents of AX to the contents of the memory location specified by based-indexed addressing mode. The opcode for the add operation is 000000.
   e) The instruction MOV WORD PTR [BP+DI+1234_H], $0ABCD_H$ says to move the immediate data word $ABCD_H$ into the memory location specified by based-indexed addressing mode. The opcode for immediate addressing MOV instruction is 1100011 W while, byte 2 has the form of [MOD, 000, R/M].
   Express the instruction in machine code.

2. Using paging mechanism, convert the given linear address $FF1C3FFE_H$ to the corresponding physical address. Note that, the content of CR0 = $8000FC2A_H$ and CR3: $00003AFB_H$. [8 Marks]



3. Answer the following questions: [8 Marks]
   a) The six segment registers on the Pentium each have a programmer invisible "cache" register associated with them. What is the purpose of this cache?
   b) What is the purpose of bus interface unit?
   c) Which flag decides whether address for a string operation is incremented or decremented?
   d) What is the result of executing the following instruction: LDS SI, [200_H] (Hint: DS = 1200_H)?

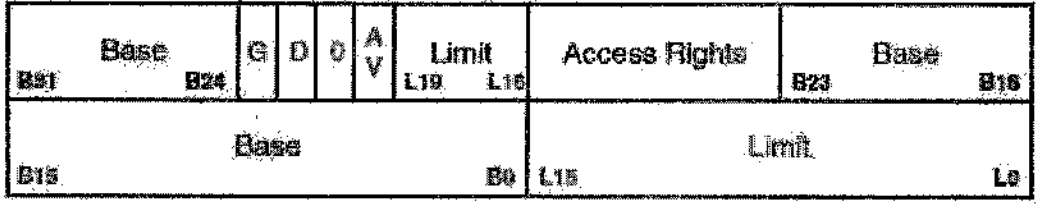
4. Assuming that register BX contains $003A_H$, what is the result of executing the following instruction: NEG BX [2 Marks]

5. Assume that prior to execution of the instruction, CL = 04, BX = 1234_H, and CF = 0. What is the result in BX and CF after execution of the following instruction: RCR BX, CL [2 Marks]

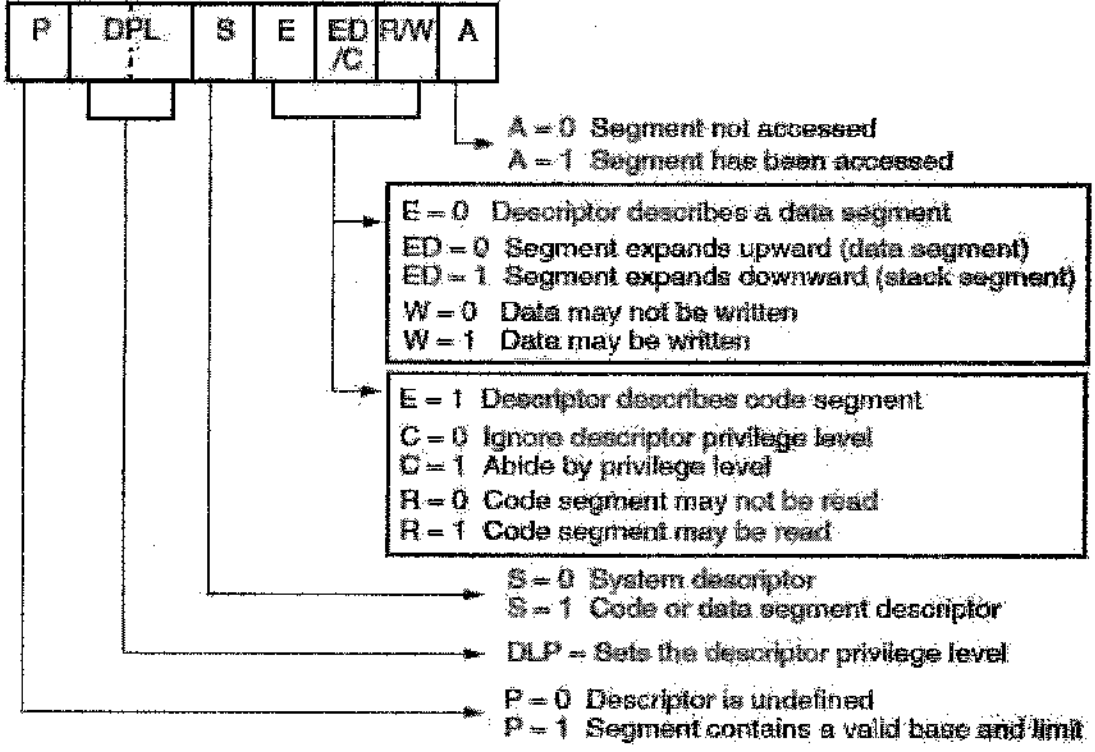
32-bit mode selected R/M | **16-bit mode selected R/M**

MOD / R/M	00	01	10	11 W=0	11 W=1	00	01	10	W=1
000	EAX	EAX+d8	EAX+d32	AL	EAX	[BX+SI]	[BX+SI+d8]	[BX+SI+d16]	AX
001	ECX	ECX+d8	ECX+d32	CL	ECX	[BX+DI]	[BX+DI+d8]	[BX+DI+d16]	CX
010	EDX	EDX+d8	EDX+d32	DL	EDX	[BP+SI]	[BP+SI+d8]	[BP+SI+d16]	DX
011	EBX	EBX+d8	EBX+d32	BL	EBX	[BP+DI]	[BP+DI+d8]	[BP+DI+d16]	BX
100	Scale index	Scale index +d8	Scale index +d32	AH	ESP	[SI]	[SI+d8]	[SI+d16]	SP
101	d32	EPB+d8	EPB+d32	CH	EBP	[DI]	[DI+d8]	[DI+d16]	BP
110	ESI	ESI+d8	ESI+d32	DH	ESI	d16	[BP+d8]	[BP+d16]	SI
111	EDI	EDI+d8	EDI+d32	BH	EDI	[BX]	[BX+d8]	[BX+d16]	DI

80386/80486/Pentium/Pentium Pro descriptor



The access rights byte for the 80286 through Core2 descriptor.



Segment register prefix override

Segment Reg.	ES	CS	SS	DS	FS	GS
Prefix Override	26H	2EH	36H	3EH	64H	65H

The scaled-index byte