Kafrelsheikh University
Faculty of Engineering
Electronics and Com. Branch
Subject: Electronic Engineering
Instructor: Dr. Bedir B. Yousif



Date: 14-1-2019 Time allowed: 3 hours Full mark: 70 Mark

Final term Exam: Two pages Academic No.: ECE2102

• Books & notes are not allowed.

Second year, First semester

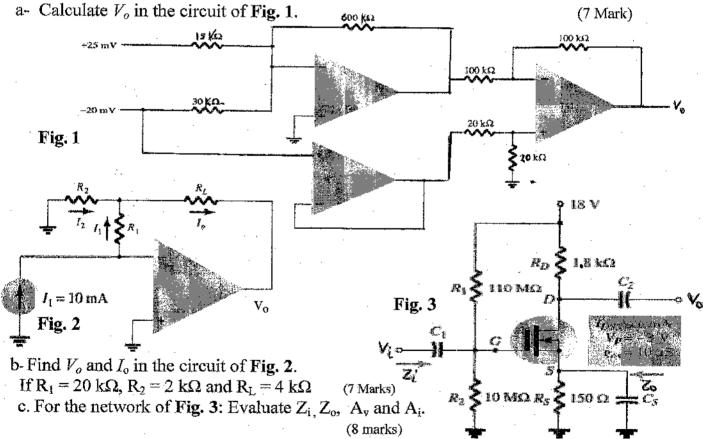
* Any missing data could be reasonably assumed.

(مخرجات التعلم المستهدفة من مقرر الهندسة الالكترونية)Course ILOS

Field	National Academic Reference Standards (NARS)			
	Knowledge & Understanding	Intellectual Skills	Professional Skills	General Skilis
Academic standards that the course contribute in achieving it	a3, a4,a5,a8 ,a14	b2, b6, b8, b16	e2,c3	d1,d7

Solve all the following questions:-

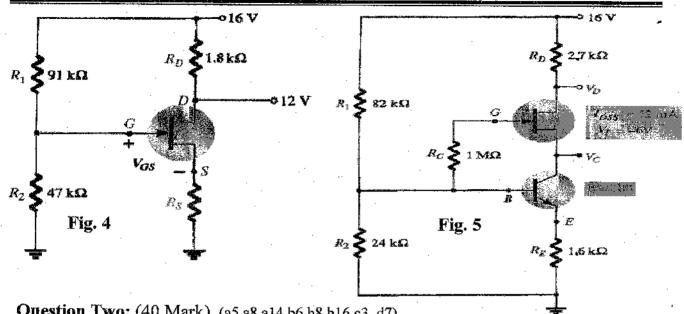
Question One: (30 Mark) (a3,a4,b2,c2,d1)



d. For the voltage-divider bias configuration

of Fig. 4, if $V_D = 12 \text{ V}$, $V_{GSoff} = -3.78 \text{ V}$ and $I_{DSS} = 10 \text{ mA}$, calculate the value of R_S .

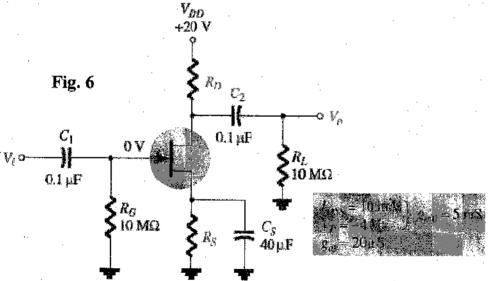
(8 marks)



Question Two: (40 Mark) (a5,a8,a14,b6,b8,b16,c3, d7)

a- Determine the levels of V_D and V_C for the network of Fig. 5. (10 marks)

b-Choose the values of R_D and R_S for the network of Fig. 6 that will result in a gain of 8 using a relatively high level of g_m for this device defined at $V_{GSQ} = \frac{1}{4}V_P$. (10 marks)



- c-Implement a boolean logic function Y=\overline{AB} +C using CMOS transistors? (7 marks)
- e- An analog switch is used to sample a signal x(t)=10+5cos2000t+8cos 8000t. Determine the minimum frequency of the pulses applied to the MOSFET gate. (5 marks)
- f. Design an analog time division multiplexer for a four input sinusoidal signals with frequencies of f_1 =5 kHz, f_2 =10 kHz, f_2 =15 kHz and f_2 =20 kHz, and peak amplitude 3 V to be transmitted on the line? Furthermore draw the input output waveforms and gating rectangular signal of 40KHz? Hint: MOSFET device has $V_{GS(th)}$ =2 V and lossless (8 marks)

Best wishes of success Dr. Bedir yousif