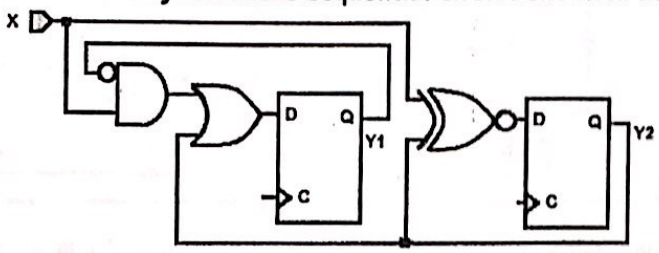
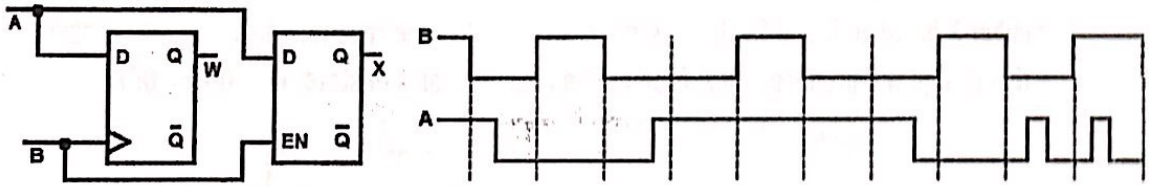
The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

QUESTION NUMBER ONE [25 MARKS]

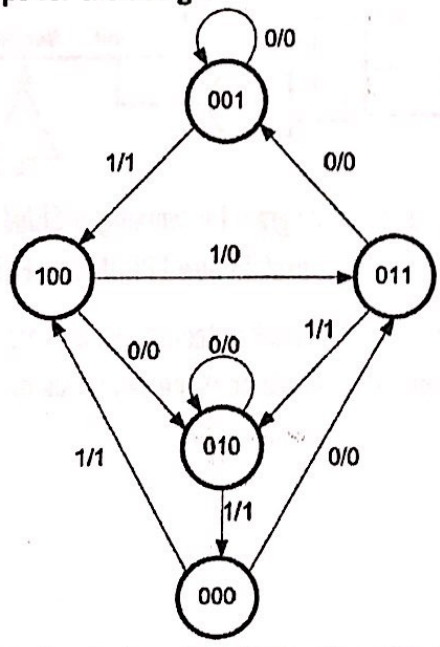
1. Write the state table for the synchronous sequential circuit shown in below figure. [5 Marks]



2. Fill in the timing diagrams for each of the following circuits. [5 Marks]



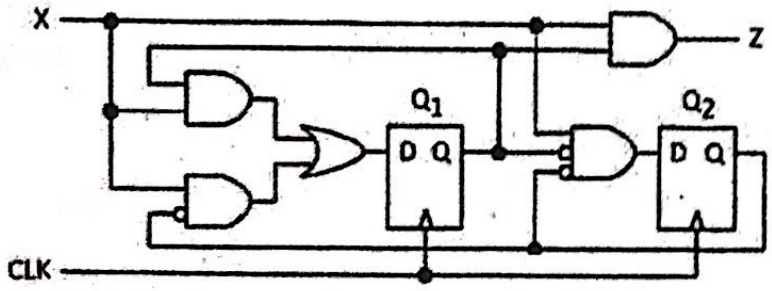
3. A sequential circuit has three flip-flops, A, B, C; one input X, and one output, Y. The state diagram is shown below. The circuit is designed by treating the unused states as don't care conditions. The final circuit must be analyzed to ensure that it is self-correcting. Use JK flip-flops for the design. [10 Marks]



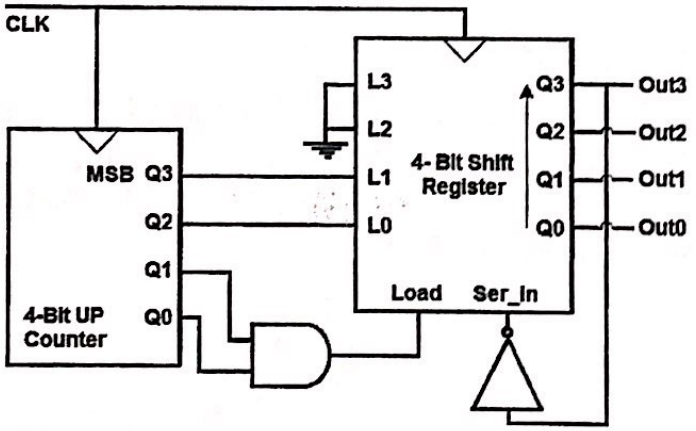
4. Write the VHDL code for the circuit describes D flip-flop with asynchronous reset. [5 Marks]

Question Number Two [35 Marks]

1. For the following clocked sequential circuit with one input (X) and one output (Z):
   a) Drive a state table and draw a state diagram for the circuit.
   b) Redesign this circuit by replacing the Q_1 flip-flop (i.e. the D flip-flop holding Q_1 state) with a JK flip-flop, and the Q_2 flip-flop with a T flip-flop. [10 Marks]



2. Consider the design below, constructed with one up-counter and one parallel input serial output shift right register. Let outputs Out3 - Out0 be the binary representation of a number X between 0 and 15 (Out3 is the MSB). What is the repeating sequence of numbers X this design will produce? Hint: Assume the counter starts in state Q3 – Q0 = 0011. [5 Marks]



3. Briefly illustrate by means of a circuit diagram the working of SRAM. Then, explain how DRAM refreshment is performed? After that, explain how EPROM and EEPROM differ. [10 Marks]

4. We wish to design a sequence detector, which detects three or more consecutive 1's in a string of bits coming through an input line. Implement the circuit using J-K flip-flops. [10 Marks]