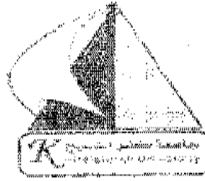


Bedir Yousif

Kafrelsheikh University
Faculty of Engineering
Department of electrical eng.
Year: 2nd Subject: Electronic eng.
Examiner: **Dr. Bedir Bedir Yousif**



Date: 14/1/2017
Time allowed: 3 Hours
Full mark: 70 Mark
Final term: Two pages
Academic Number: ECE2103

Solve the following questions:-

Question One (20 Mark)

1. Determine the output voltage for the circuit in Fig. 1, (6 marks)

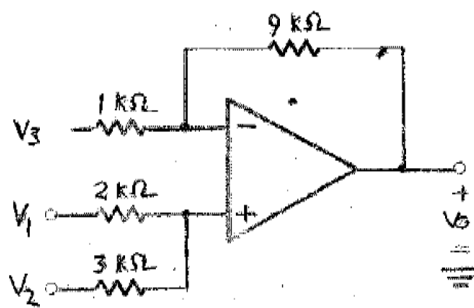


Fig . 1

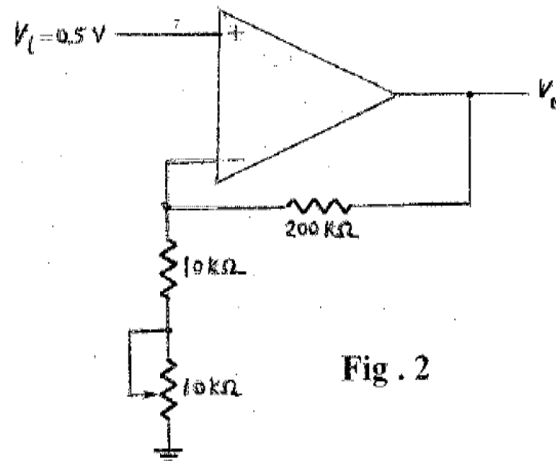


Fig . 2

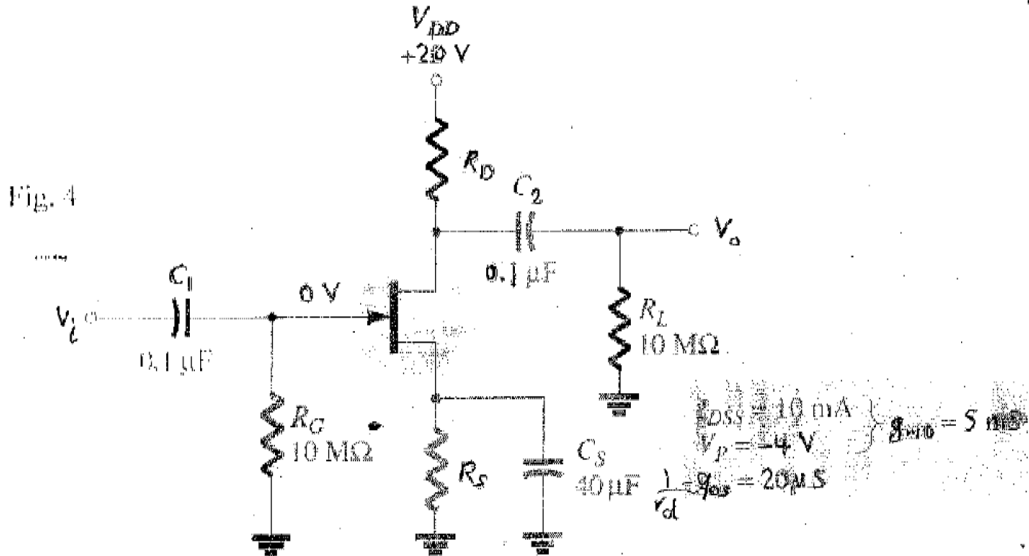
2. What range of output voltage is developed in the circuit of Fig. 2 (7 marks)
3. Define CMRR and how to experimentally measure CMRR? (7 marks)

Question Two (30 Mark)

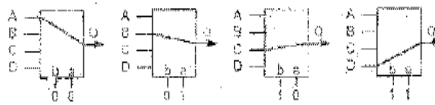
1. Calculate the efficiency of a class B amplifier for a supply voltage of $V_{CC} = 22\text{ V}$ driving a $4\ \Omega$ load with peak output voltages of: a. $V_L(p) = 20\text{ V}$ b. $V_L(p) = 4\text{ V}$.
2. A transformer-coupled class A amplifier drives a $16\text{-}\Omega$ speaker through a $3.87:1$ transformer. Using a power supply of $V_{CC} = 36\text{ V}$, the circuit delivers 2 W to the load. Calculate:
a. $P(ac)$ across transformer primary.
b. $V_L(ac)$.
c. $V(ac)$ at transformer primary.
d. The rms values of load and primary current.
3. Explain briefly three different configurations of practical class B power amplifier

Question Three (30 Mark)

- 1- Choose the values of R_D and R_S for the network of Fig. 3 that will result in a gain of 8 using a relatively high level of g_m for this device defined at $V_{GSQ} = 0.25V_P$.



- 2- An analog switch uses an n-channel MOSFET with $V_{GS(th)} = 4$ V. A voltage of +8 V is applied to the gate. Determine the maximum peak-to-peak input signal that can be applied if the drain-to-source voltage drop is neglected.
- 3- An analog switch is used to sample a signal with $x(t) = 10 + 5 \cos 2000t + 8 \cos 8000t$. Determine the minimum frequency of the pulses applied to the MOSFET gate.
- 4- Design a quad time division multiplexer using an n-channel MOSFET with $V_{GS(th)} = 3$ V. A voltage of +8 V is applied to the gate of each MOSFET during $0.25 \mu s$. Calculate the sampler frequency and maximum signal frequency.



Best wishes of success
Dr. Bedir yousif

$$V = 2 \times \frac{V_2}{5} (1+9) = 4V_2$$

$$\Rightarrow \frac{3V_1}{5} (1+9) = 4V_2$$