Kafrelsheikh University
Faculty of Engineering
Electrical Engineering Department
Final Exam, 2018 - 2019
Subject: Computer Architecture.



Year: 3th Computer Engineering & systems

Academic Number : ECS3009 Date: 16 / 1 / 2019

Date: 16 / 1 / 2019 Time: 3 Hours.

Full Mark: 60, 2 pages

This exam measures ILOs no: a3, a4, a8, a13, a14, b4, b5 b6, b13, c3, c6, c14, d1, d4

Question #1: Answer briefly on the following questions [20 Marks]

- 1. What, in general terms, is the distinction between computer organization and computer architecture?
- 2. What is the difference between RISC and CISC? Give example for each.
- 3. Discus the different between direct and indirect addressing modes? Use drawing whenever you can.
- 4. Mention the instruction cycle.
- 5. Discuss in briefly, the types of ROM.
- 6. What is a pipeline hazard? What are their types?
- 7. Compare between SRAM & DRAM.
- 8. List the techniques used for overcoming hazard.
- 9- What are the modes of I/O transfer data? Discuss briefly
- 10- What is a priority interrupt?

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Question #2: Choose the correct answer:	[5 Marks]	OR PORTING THE REPORT OF THE REAL PROPERTY OF THE R		
1- Execution of a Program in the Von Neuma a. Concurrently b. Randomly c. Seq	ann system is done quentially d. None of the	se market work (d)		
2- In IEEE 32-bit representations, the mantis a. 24 b. 23 c. 20	ssa of the fraction is said t d. 16	o occupy bits.		
3- Given set of instructions add \$\$50, \$\$t0, \$\$t1; sub \$\$t2, \$\$50, \$\$t3; shows:				
a. Structural hazards b. Data hazards	c. forwarding bypassing	d. Pipeline stall		
4- In CISC architecture most of the complex instructions are stored in				
a. Register b. Diodes	c. CMOS	d. Transistors		
5- A data bus is				
a. Bidirectional c. Provid	c. Provides path for moving data between system modules			
b. Transfers bits of a word in parallel d. All of above				

Question #3: Answer by explanations the following questions [25 Marks]

1- Design a 3-bit binary ALU operations due to the following truth table of the control signals.

[5 Marks]

S1	S2	operation
0	0	A OR B
0	1	A AND B
1	0	A XOR B
1	1	A+B

- 2- Use the Booth algorithm to multiply 23 (multiplicand) by 29 (Multiplier), where each number is represented using 6 bits. [4 marks]
- 3- Carry out the calculation steps for 4-bit binary division of positive numbers 1001/0100 (i.e., 9/4) using the division algorithm.
- 4- Show the IEEE 754 binary representation for the following floating-point numbers in single precision 356.75. [4 marks]
- $y = 0\ 100\ 0100\ 1\ 001\ 0100\ 1000\ 0000\ 0000\ 0000$

With these single precision IEEE 754 floating- point numbers, perform, showing all work:

a) x+v b) x*v

[8 marks]

Question #4: Pipeline [10 marks]

Consider the following sequence of instructions being processed on the pipelined 5-stage RISC processor. Assume that this pipeline does not use operand forwarding. Also, assume that the only sources of pipeline stalls are the data hazards.

> Add R4, R2, R3 Store R5, #100(R4) Load R6, #200(R4) Subtract R7, R5, R6

- (a) Draw a diagram that represents instruction flow through the pipeline during each clock cycle. How long does it take for the instruction sequence to complete?
- (b) Now, assume that the pipeline uses operand forwarding. There are separate forwarding paths from the outputs of stage-3 and stage-4 to the input of stage-3. Draw a diagram that represents the flow of instructions through the pipeline during each clock cycle. Indicate operand forwarding by arrows.

********** With Best Wishes **********

Dr. Wessam Fikry, Committee of Correctors and Testers