KAFR-ELSHIEKH UNIVERSITY
FACULTY OF ENGINEERING
TIME ALLOWED: 3 HOURS

ELECTRICAL ENGINEERING DEPARTMENT
COMPUTER ENGINEERING AND SYSTEMS BRANCH
2ND YEAR FINAL EXAM OF 1ST SEMESTER 2017 - 2018
MICROPROCESSOR SYSTEMS [CODE NO. ECS 2006]

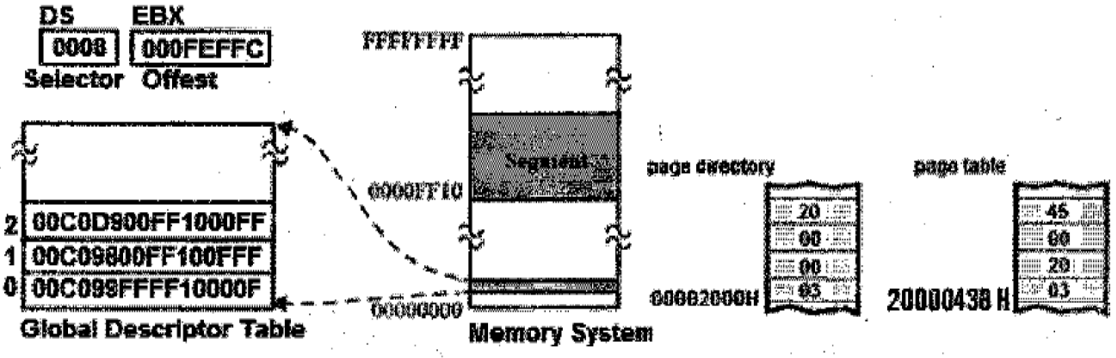
The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

QUESTION NUMBER ONE [30 MARKS]

1. Compatibility between the later and earlier microprocessors has been a successful strategy for the Intel family. Give two distinct examples of the modifications that demonstrate this compatibility. Afterwards, mention the elements which effect of microprocessor performance speed. [5 Marks]

2. Show an example of subtracting two 7-bit signed numbers that result in an overflow, thus rendering the final 7-bit difference invalid. Show both the numbers being subtracted and the resulting invalid difference. [2 Marks]

3. Write descriptive note on paging; explain how it is used for memory addressing. After that, use the descriptor definition to calculate the appropriate linear address. If the microprocessor sends this linear address to the paging mechanism, which memory segment is accessed (Assume CR3 contains 00002H)? Justify your answer. [12 Marks]



4. What is the address of next instruction for the following (justify your answer): [4 Marks]
   a) 0B03 : 0106 7218 JC 0120H
   b) If JC is replaced with JO, what is the address of the next instruction?
   Debug screen: OV UP EI NG NZ NA PO NC

5. What is the use of these assembler directives? [3 Marks]
   a) DB b) .MODEL tiny

6. Mention how the following instructions differ in their functionality: [4 Marks]
   a) NEG & NOT b) DIV & IDIV
   c) AND & TEST d) CMP & SUB

Question Number Two [30 Marks]

1. In Intel 8086 microprocessor, why is the segment register content appended by "0" to generate the physical address? What are the maximum number of non-overlapping segment for Intel 80386 microprocessor operated in the real and protect modes? [4 Marks]

2. Which of the following instruction is a correct assembly instruction and which is not? Why? Correct if possible. [6 Marks]

   a) MOV AL, [SI+DI] b) PUSH AL c) INC [SI]
   d) ADD [0100H], [0220H] e) MOV BL, [CX] f) ADD BX, AL

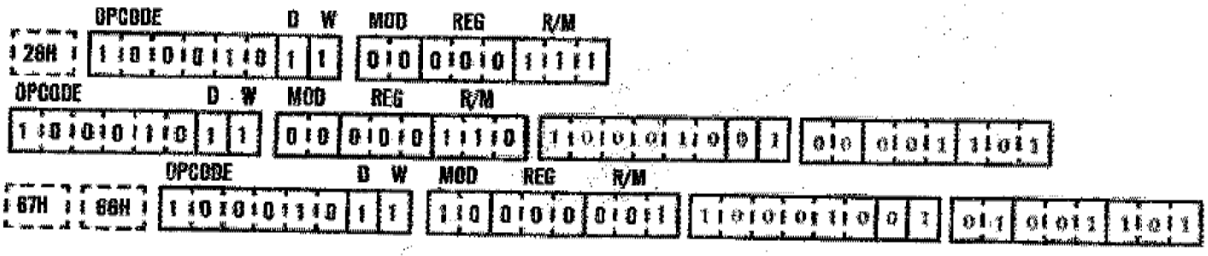
3. Swap the word at memory location 24000H with 25000H. Next, write an assembly language program to find the largest signed number from a set of 10 bytes stored at array. The greatest number must be stored at location RES. [7 Marks]

4. Write a single logical instruction for each of the following operations. Note that, no other changes should occur. [5 Marks]

   a) Set the most significant nibble in AX to 1;
   b) Clear the even numbers bits in AX to 0;
   c) Invert bit number 0, 5, 10, and 15 in AX;
   d) Change the sign of the content of AX;
   e) Multiply the content of AX by 16.

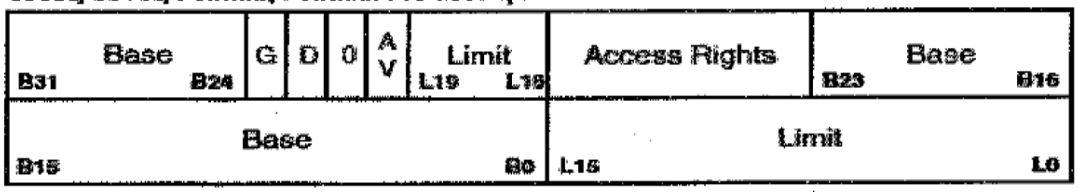
5. Describe how the LDS BX, NUMB instruction operates. [2 Marks]

6. Mention at least 4-types of data addressing modes (use examples to illustrate your answer). Henceforth, give the assembly instruction encoded by the following: [6 Marks]

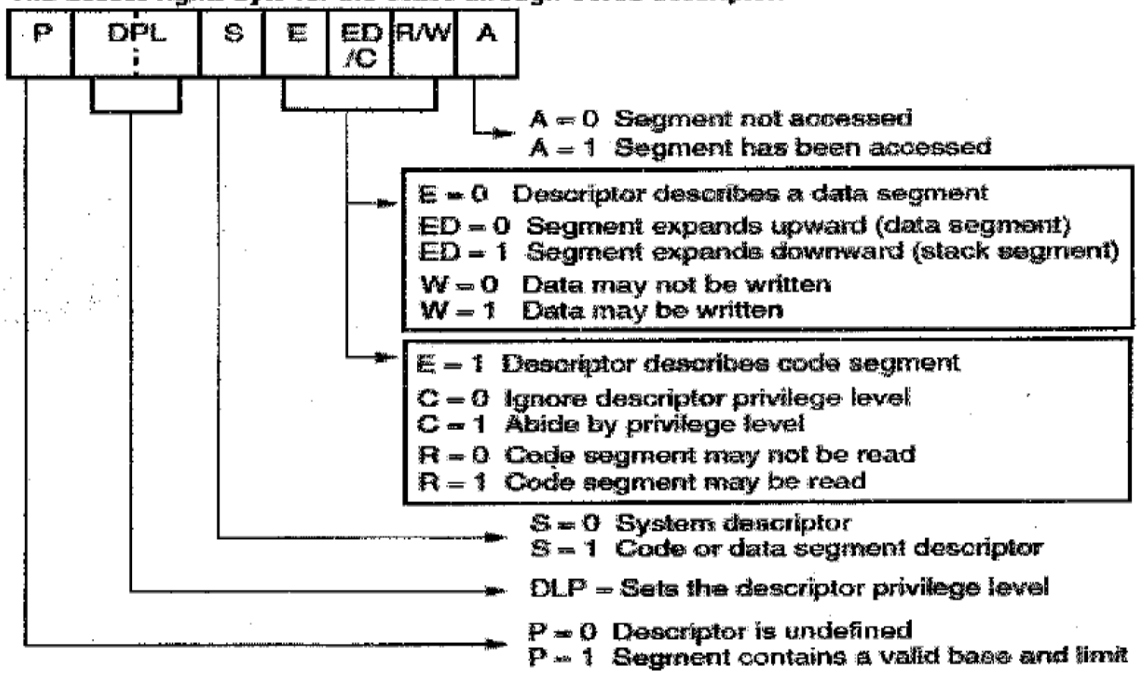


32-bit mode selected R/M						16-bit mode selected R/M			
MOD / R/M	00	01	10	11 W=0	11 W=1	00	01	10	W=1
000	EAX	EAX+d8	EAX+d32	AL	EAX	[BX+SI]	[BX+SI+d8]	[BX+SI+d16]	AX
001	ECX	ECX+d8	ECX+d32	CL	ECX	[BX+DI]	[BX+DI+d8]	[BX+DI+d16]	CX
010	EDX	EDX+d8	EDX+d32	DL	EDX	[BP+SI]	[BP+SI+d8]	[BP+SI+d16]	DX
011	EBX	EBX+d8	EBX+d32	BL	EBX	[BP+DI]	[BP+DI+d8]	[BP+DI+d16]	BX
100	Scale index	Scale index +d8	Scale index +d32	AH	ESP	[SI]	[SI+d8]	[SI+d16]	SP
101	d32	EPB+d8	EPB+d32	CH	EBP	[DI]	[DI+d8]	[DI+d16]	BP
110	ESI	ESI+d8	ESI+d32	DH	ESI	d16	[BP+d8]	[BP+d16]	SI
111	EDI	EDI+d8	EDI+d32	BH	EDI	[BX]	[BX+d8]	[BX+d16]	DI

80386/80486/Pentium/Pentium Pro descriptor



The access rights byte for the 80286 through Core2 descriptor.



Segment register prefix override

Segment Reg.	ES	CS	SS	DS	FS	GS
Prefix Override	26H	2EH	36H	3EH	64H	65H