KAFR-ELSHEIKH UNIVERSITY
FACULTY OF ENGINEERING
TIME ALLOWED: 3 HOURS

ELECTRICAL ENGINEERING DEPARTMENT
COMPUTER ENGINEERING AND SYSTEMS BRANCH
1ST YEAR FINAL EXAM OF 1ST SEMESTER 2017 - 2018
LOGIC CIRCUITS [CODE NO. ECS 1004]

The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

- Clarify your answer with the suitable sketches as you can.
- Please use a pen or heavy pencil to ensure legibility.
- Please attempt all questions.

QUESTION NUMBER ONE [25 MARKS]

1. Give the possible rang of values of the signed integer N, such that when 8-bit binary number N is adding to signed integer 53H, we have no overflow. Likewise, give the possible values of the 8-bit binary number N that when you add to the positive number 48H the sign bit of the result is 1 and overflow bit is equal 0. [6 Marks]

2. Using the least number of 4-bit binary adders and gates, design a BCD adder/subtractor. The adder/subtractor should receive two 4-bit numbers and should produce 4-bit sum/difference and a carry/borrow output. [6 Marks]

3. The circuit in Fig. 1 is used to implement the function Z, *i* and j can be selected from the set {0, 1, B, $\overline{B}$}. What values should be chosen for *i* and j? [3 Marks]

$$Z = f(A, B) = A + B$$

4. Fig. 2 shows a logic circuit with four full-adders. Two 4-bit integers $Y=Y_3\ Y_2\ Y_1\ Y_0$ and X= X3 X2 X1 X0 are added with each other in this circuit. Assume that Y= 0111 what is the value at X when Z=1? What is then the value of C4? [3 Marks]

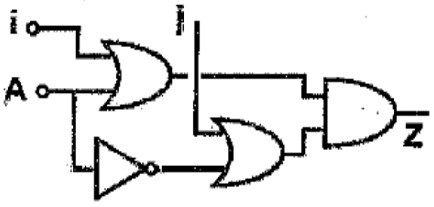


Fig. 1

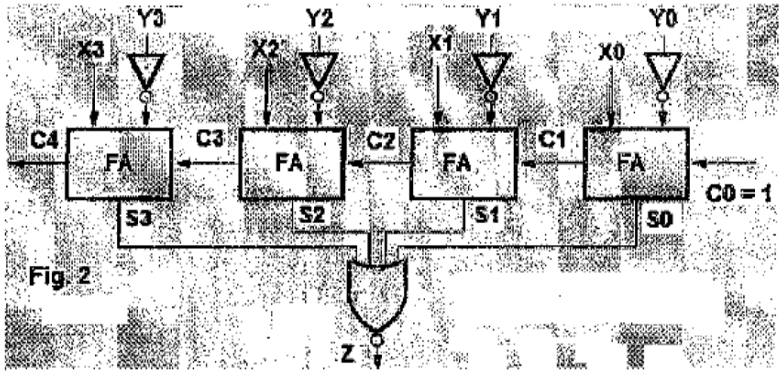
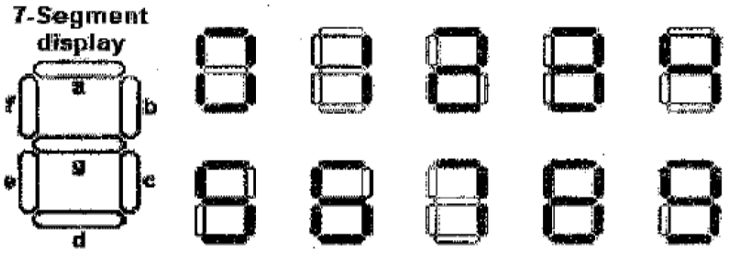


Fig. 2

5. Given X (dividend) = 0111 and M (divisor)=0011, show the contents of A and Q registers during the process of division. After that, provide a circuit diagram showing how to implement XOR gate using NAND gate. [7 Marks]

QUESTION NUMBER TWO [35 MARKS]

1. One older device has a 7-segment display with 7-light bulbs, but it lacks an outlet for connection to a computer. One could therefore need a combinatorial circuit that connects to the bulbs and then converts 7-segment code to the usual BCD code that is used by a variety of other equipments. Design BCD to 7-segment decoder, using a minimum number of gates. The six invalid combinations should result in a blank display. [8 Marks]



2. What are the advantages of minimizing logic circuits? After that, draw the minimum NAND implementation for F(A,B,C,D).

$$F(A, B, C, D) = \Sigma m(1,5,8,13,14,15) + D(3,10,12)$$

Next, by using Boolean algebra prove that: $A + \overline{A}B + A\overline{B} = A + B$. [7 Marks]

3. There is an error in Fig. 3 that is used to implement of the carry out logic. Identify the error and propose a simple solution. Afterwards, complete the truth table realized by the given multiplexer circuit shown in Fig. 4. Next, derive the K-map for this logic function. Realize the function minimized with the use of PLA. [8 Marks]

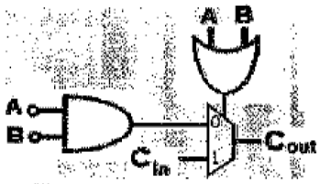


Fig. 3

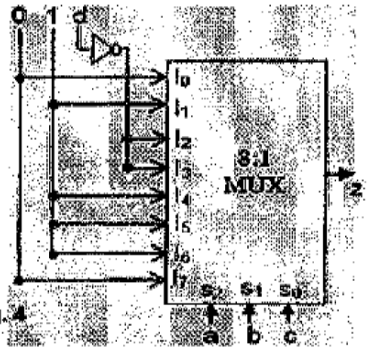


Fig. 4

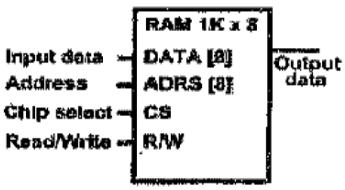


Fig. 5

4. Suppose that we want to construct 4K x 8 bit RAM by using 1 K x 8 bit RAM chips illustrated in Fig. 5. Draw the block diagram that illustrates the interconnection of the necessary number of chips to form a 4 K x 8 bit RAM. [6 Marks]

5. Write the VHDL code for the circuit describes a 4-to-1 multiplexer. [6 Marks]