KAFR-ELSHIEKH UNIVERSITY
FACULTY OF ENGINEERING
TIME ALLOWED: 3 HOURS

ELECTRICAL ENGINEERING DEPARTMENT
COMPUTER ENGINEERING AND SYSTEMS BRANCH
2ND YEAR FINAL EXAM OF 2ND SEMESTER 2017 - 2018
MICROPROCESSOR SYSTEMS [CODE NO. ECS 2006]

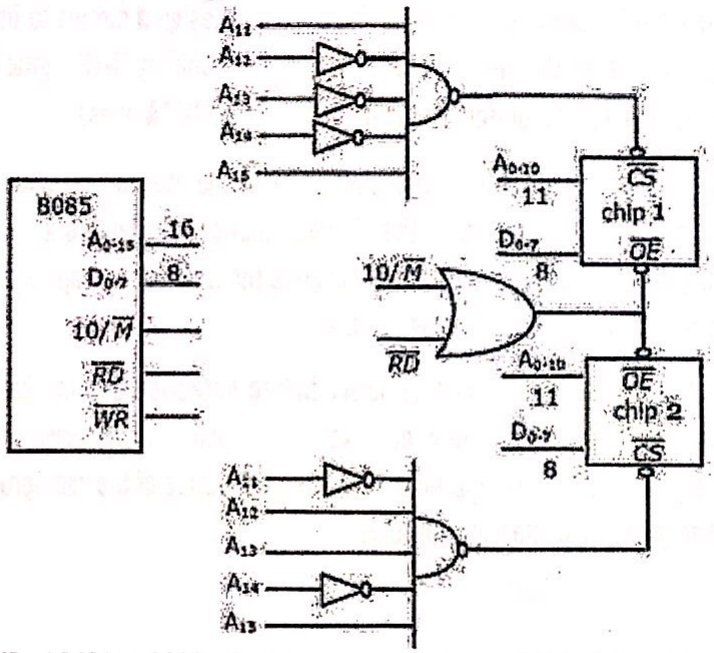
The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

- Clarify your answer with the suitable sketches as you can.
- Please use a pen or heavy pencil to ensure legibility.
- Please attempt all questions.

QUESTION NUMBER ONE [20 MARKS]

1. Briefly illustrate by means of a circuit diagram the working of DRAM. Then, explain how DRAM refreshment is performed? After that, explain how FAMOS and FLOTOX memory devices differ. [6 Marks]
2. The following figure shows the memory circuit of 8085 microprocessor.
   a) What is the total size of the memory in the circuit?
   b) What are the beginning and ending addresses of the memory chips?
   c) How will you replace the two NAND gates in the circuit with one 3 to 8 decoder without changing the memory size or the memory addresses? Assume that the decoder has one active high enable E1 and one active low enable E2. [6 Marks]



3. Interface 16 KB of RAM to 8086 microprocessor starting at 00000H. Two kinds of chips available are 2KB (4 chips) and 4KB (2 Chips). [8 Marks]

QUESTION NUMBER TWO [20 MARKS]

1. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. Draw the instruction word format and indicate the number of bits in each part? How many bits are there in the data inputs of the memory? [4 Marks]
2. Explain why each of the following micro-operations cannot be executed during a single clock pulse. Specify a sequence of micro-operations that will perform the operation.
   a) IR ← M[PC]
   b) AC ← AC + TR
   c) DR ← DR + AC (AC does not change) [5 Marks]
3. What are the two instructions needed in the basic computer to set the E flip-flop to 1? [2 Marks]
4. Show the complete logic of the interrupt flip-flops R in the basic computer. Use a JK flip-flop and minimize the number of gates. [5 Marks]
5. Show the gate structure associated with the control inputs of AR. [4 Marks]

QUESTION NUMBER THREE [20 MARKS]

1. Explain how with some hardware modification it is possible to expand the INTR pin, so that it accepts seven interrupt request signals. Then, please design a circuit to implement a hardware interrupt for the interrupt vector type $F7_H$ (including INTR signal request, $\overline{\text{INTA}}$ output signal and a buffer 74LS244 to pass $F7_H$ to DATA lines). [6 Marks]
2. Does the $\overline{\text{INTA}}$ signal activate for the NMI pin? List the events that occur when a protected mode interrupt becomes active. In your answer, I expect to know how the task state segment is addressed. Afterward, describe the function of trap flag and then, write a procedure that disable trapping feature. [8 Marks]
3. Briefly illustrate the working operation of power failure detection circuit that causing NMI interrupt when AC power drop out. As a final point, write down with proper diagrams an explanatory note on expanding the interrupt structure of the microprocessor by using 82S9A programmable interrupt controller. [6 Marks]

Fetch	$R'T_0$:	$AR \leftarrow PC$
	$R'T_1$:	$IR \leftarrow M[AR]$, $PC \leftarrow PC + 1$
Decode	$R'T_2$:	$D_0, \ldots, D_7 \leftarrow$ Decode $IR(12\text{–}14)$, $AR \leftarrow IR(0\text{–}11)$, $I \leftarrow IR(15)$
Indirect	D_7IT_3:	$AR \leftarrow M[AR]$
Interrupt:		
	$T_0'T_1'T_2'(IEN)(FGI + FGO)$:	$R \leftarrow 1$
	RT_0:	$AR \leftarrow 0$, $TR \leftarrow PC$
	RT_1:	$M[AR] \leftarrow TR$, $PC \leftarrow 0$
	RT_2:	$PC \leftarrow PC + 1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$
Memory-reference:		
AND	D_0T_4:	$DR \leftarrow M[AR]$
	D_0T_5:	$AC \leftarrow AC \wedge DR$, $SC \leftarrow 0$
ADD	D_1T_4:	$DR \leftarrow M[AR]$
	D_1T_5:	$AC \leftarrow AC + DR$, $E \leftarrow C_{out}$, $SC \leftarrow 0$
LDA	D_2T_4:	$DR \leftarrow M[AR]$
	D_2T_5:	$AC \leftarrow DR$, $SC \leftarrow 0$
STA	D_3T_4:	$M[AR] \leftarrow AC$, $SC \leftarrow 0$
BUN	D_4T_4:	$PC \leftarrow AR$, $SC \leftarrow 0$
BSA	D_5T_4:	$M[AR] \leftarrow PC$, $AR \leftarrow AR + 1$
	D_5T_5:	$PC \leftarrow AR$, $SC \leftarrow 0$
ISZ	D_6T_4:	$DR \leftarrow M[AR]$
	D_6T_5:	$DR \leftarrow DR + 1$
	D_6T_6:	$M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$
Register-reference:		
	$D_7I'T_3 = r$ (common to all register-reference instructions)	
	$IR(i) = B_i$ $(i = 0, 1, 2, \ldots, 11)$	
	r:	$SC \leftarrow 0$
CLA	rB_{11}:	$AC \leftarrow 0$
CLE	rB_{10}:	$E \leftarrow 0$
CMA	rB_9:	$AC \leftarrow \overline{AC}$
CME	rB_8:	$E \leftarrow \overline{E}$
CIR	rB_7:	$AC \leftarrow$ shr AC, $AC(15) \leftarrow E$, $E \leftarrow AC(0)$
CIL	rB_6:	$AC \leftarrow$ shl AC, $AC(0) \leftarrow E$, $E \leftarrow AC(15)$
INC	rB_5:	$AC \leftarrow AC + 1$
SPA	rB_4:	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$
SNA	rB_3:	If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$
SZA	rB_2:	If $(AC = 0)$ then $PC \leftarrow PC + 1$
SZE	rB_1:	If $(E = 0)$ then $(PC \leftarrow PC + 1)$
HLT	rB_0:	$S \leftarrow 0$
Input-output:		
	$D_7IT_3 = p$ (common to all input–output instructions)	
	$IR(i) = B_i$ $(i = 6, 7, 8, 9, 10, 11)$	
	p:	$SC \leftarrow 0$
INP	pB_{11}:	$AC(0\text{–}7) \leftarrow INPR$, $FGI \leftarrow 0$
OUT	pB_{10}:	$OUTR \leftarrow AC(0\text{–}7)$, $FGO \leftarrow 0$
SKI	pB_9:	If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$
SKO	pB_8:	If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$
ION	pB_7:	$IEN \leftarrow 1$
IOF	pB_6:	$IEN \leftarrow 0$