Kafrelsheikh University - Faculty of Engineering			
Course	Integrated Circuits	Date	13/1/2020
Time	3 Hours	Mark	90
Students	4th year Electronics and Electrical Communications		

This exams measures ILOs: a.4, a.5, a. 8 , a.14, a.15 ,a.24,b.2, b.3, b.4 b.5 ,b.8, b.9, b13,c.3,c.17, d.7

Answer all the following questions:

Clarify your answer with the suitable diagrams.

Q1. Define with drawings the following terms. (15 Marks)

Propagation delay t_P. b- Rise time t_r c- Fall time t_f

Then explain how the delay is measured using the ring oscillator.

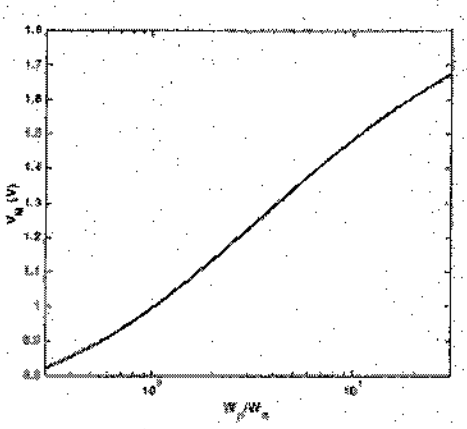
Q2.a Explain the channel capacitance of the MOSFET. (5 Marks)

Q2.b a Assume a wafer size of 42 inch, a die size of 10 cm2, 1 defects/cm2, and $\propto = 3$. Determine. A-the number of dies per wafer. B- the die yield of this CMOS process run. (10 Marks)

Q3.a Draw the Static CMOS inverter and State its properties. (5 Marks)

Q.3b Explain the skin effect in the wires of the integrated circuits. (10 Marks)

Q4.a The following is the curve of the simulated inverter switching threshold the Static CMOS inverter.

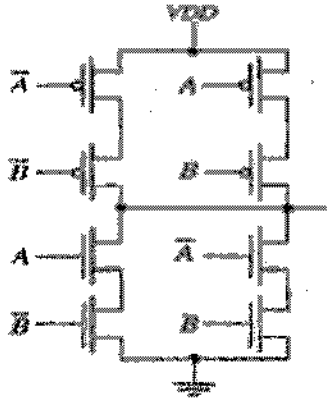


Explain when it is desirable in some application to changing the Wp/Wn ratio. (5 Marks)

Q4.b Explain the effect of Scaling the Supply Voltage on the Robustness of the CMOS inverter. **(10 Marks)**

Q5.a Explain why in the Complementary CMOS, the PDN is constructed using NMOS devices, while PMOS transistors are used in the PUN. **(5 Marks)**

Q 5.b Find the logic expression for the following static CMOS gate. **(10 Marks)**



Verify your Answer with the truth table.

Q6.a Explain the advantages and disadvantages of the Differential Pass Transistor Logic (5 Marks)

Q5.b Draw and Explain how the Differential Cascode Voltage Switch Logic (or DCVSL) works including its advantages over the pseudo-NMCS logic gate. **(10 Marks)**

Good Luck and Best Wishes ***Dr. Ibrahim Elashry***