The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

- Clarify your answer with the suitable sketches as you can.
- Please use a pen or heavy pencil to ensure legibility.
- Please attempt all questions.

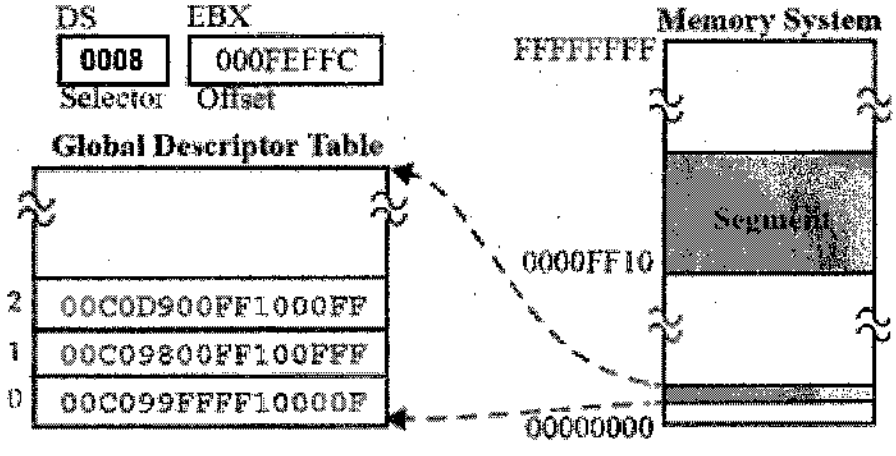
QUESTION NUMBER ONE [35 MARKS]

1. With neat block diagram explain architecture of 8086 microprocessor. Then, explain the various string related instructions in 8086 microprocessor. [9 Marks]

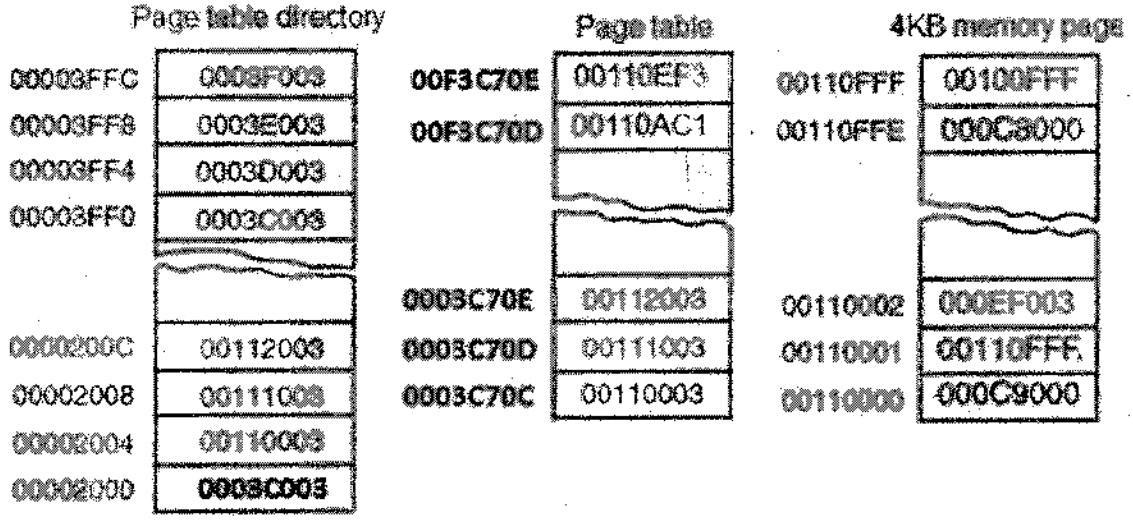
2. Assume the values of the following registers are: CS= 1000H, SS= 2000H, DS= 3000H, ES= 4000_H, SP=0002_H, BP=0000_H, BX=0001_H, SI= 0001_H, and DI= 0001_H, what is the physical address of a memory accessed by the following instructions (if it is word, give the address of the 1st and 2nd bytes). Will one of the following instructions override the data in the memory by another one? Why? [6 Marks]

   a) MOV [BX], AL
   b) [BP], CX
   c) PUSH DX
   d) MOV [BX+SI], AL

3. Code a descriptor that describes a memory segment that begins at location 210000_H and ends at location $21001F_H$. This memory segment is a code segment that can be read. The descriptor is for an 80286 microprocessor. After that, use the descriptor definition to decode the appropriate descriptor shown in below figure. [10 Marks]

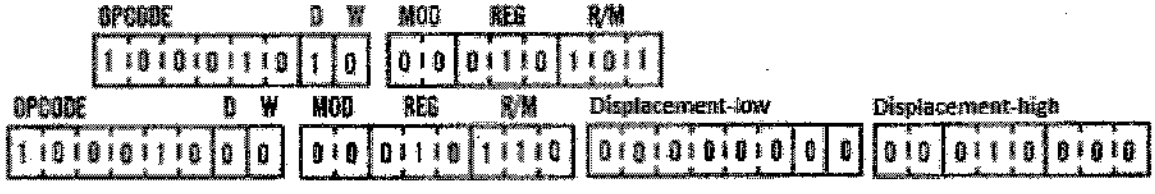


4. If the 80386 microprocessor sends linear address $FF1C3FFE_H$ to the paging mechanism, explain how 32-bit physical address is generated with paging enable. Note that, the content of CR0=$8000FC2A_H$ and CR3= $00003AFB_H$. [10 Marks]



QUESTION NUMBER ONE [25 MARKS]

1. If BH =72 and DH = FF, list the contents of each register and the contents of each flags after the following tasks: a) XADD BH, DH, and b) CMPXCHG BH, DH. [4 Marks]
2. Select the correct instruction to perform each of the following tasks:
   a) Invert the leftmost 10 bits of BX register without changing the rightmost 6 bits.
   b) Move the DH register right one place, making sure that the sign of the result is the same as the sign of the original number. [4 Marks]
3. What is the purpose of the direction flag? Hereafter, describe how the "LODSW" instruction operates. Assume that D=0. SI=1000, and DS=1000. [4 Marks]
4. What registers are placed on the stack by the PUSHA instruction? In what order? [3 Marks]
5. Compare the operation of MOV DI, NUMB instruction with LEA DI, NUMB instruction. [3 Marks]
6. Is it possible to have two different machine codes for the same instruction? Give the assembly instruction encoded by the following:



If MOV EAX, [EBX+4*ECX] appears in a program for the Pentium microprocessor operated in the 16-bit mode, what is its machine language equivalent? [7 Marks]

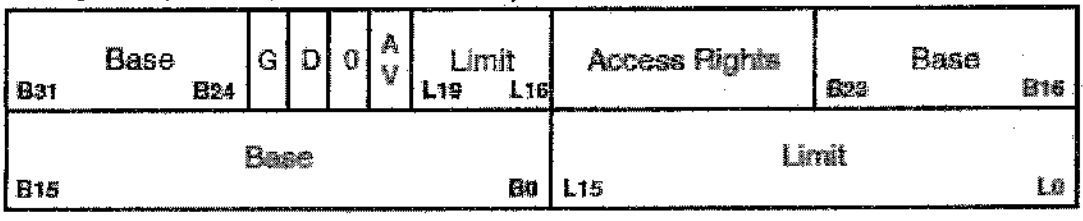
32-bit mode selected R/M

MOD / R/M	00	01	10	11 W=0	11 W=1
000	EAX	EAX+d8	EAX+d32	AL	EAX
001	ECX	ECX+d8	ECX+d32	CL	ECX
010	EDX	EDX+d8	EDX+d32	DL	EDX
011	EBX	EBX+d8	EBX+d32	BL	EBX
100	Scale index	Scale index +d8	Scale index +d32	AH	ESP
101	d32	EPB+d8	EPB+d32	CH	EBP
110	ESI	ESI+d8	ESI+d32	DH	ESI
111	EDI	EDI+d8	EDI+d32	BH	EDI

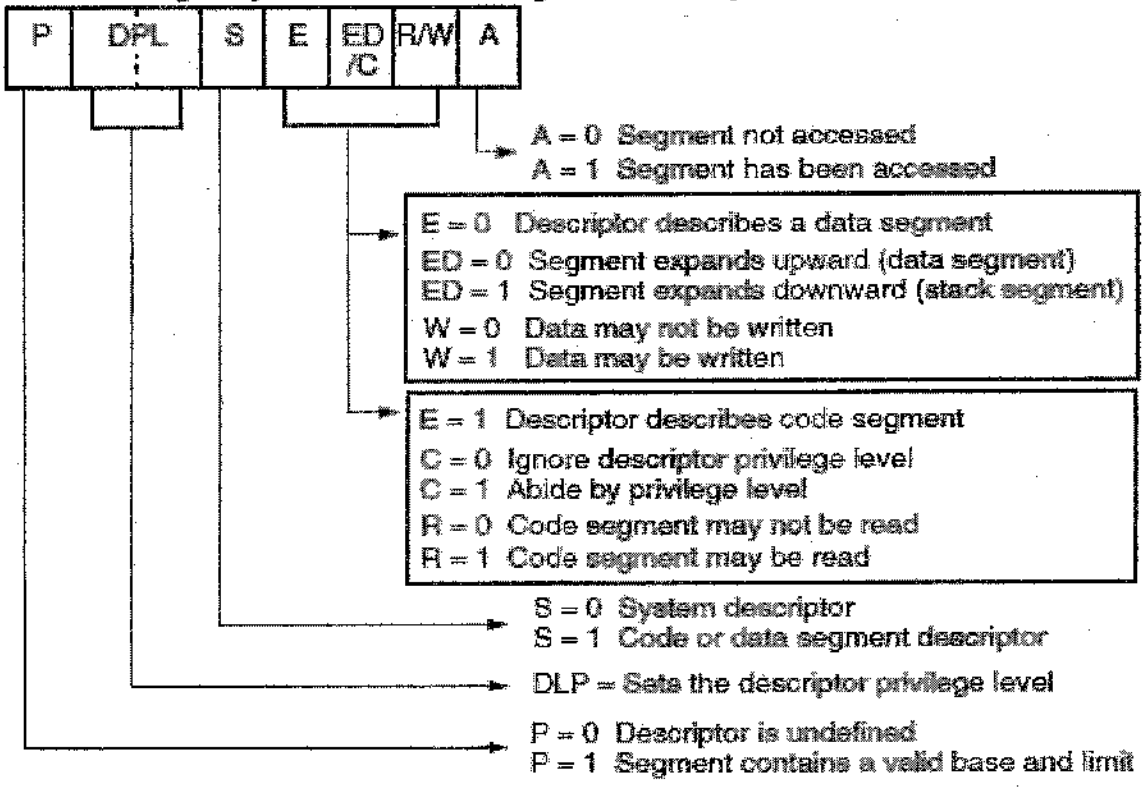
16-bit mode selected R/M

00	01	10	W=1
[BX+SI]	[BX+SI+d8]	[BX+SI+d16]	AX
[BX+DI]	[BX+DI+d8]	[BX+DI+d16]	CX
[BP+SI]	[BP+SI+d8]	[BP+SI+d16]	DX
[BP+DI]	[BP+DI+d8]	[BP+DI+d16]	BX
[SI]	[SI+d8]	[SI+d16]	SP
[DI]	[DI+d8]	[DI+d16]	BP
d16	[BP+d8]	[BP+d16]	SI
[BX]	[BX+d8]	[BX+d16]	DI

80386/80486/Pentium/Pentium Pro descriptor



The access rights byte for the 80286 through Core2 descriptor.



Segment register prefix override

Segment Reg.	ES	CS	SS	DS	FS	GS
Prefix Override	26H	2EH	36H	3EH	64H	65H

The scaled-index byte