Ministry of Higher Education and Scientific Research Faculty of Engineering Kafrelsheikh University	كلية الهندسة	وزارة التعليم العالي والبحث العلمي كلية الهندسة جامعة كفر الشيخ
Final-term Examination of Academic Year 2019/2020		
Department: Electrical Engineering	**Year: second year**	**Total Marks: 70**
Course Title: Electrical Engineering	**Course Code: ECE 2102**	**Term: First Term**
Date: Jan. 13 - 2020	**Number of questions: 6**	**Allowed Time: 180** Minutes

Answer the following questions

Illustrate your answers with sketches when necessary

Question 1 **(10 Marks)**

For the circuit of Fig. 1, find the DC collector currents of both Q_1 and Q_2 given that $R = 10k\Omega, \beta = 100, V_{cc} =$ 15 V and $I_{co3} = 3\ I_{co4}$

Question 2 **(20 Marks)**

A. Drive the amplifier parameters (input impedance, output impedance, and overall voltage gain) of the circuit shown in figure 2. (10 Marks)

B. Design the bias circuit of the CE amplifier of Fig. 2 to obtain $I_E = 0.5\ mA$, $V_C = 6\ V$, dc voltage at the base of 5 V, and a current through R_{B2} of 50 μA. Let $V_{CC} = 15\ V, \beta = 100$, and $V_{BE} = 0.7\ V$. Find the amplifier parameters when $R_{sig} = 10\ k\Omega\ , R_e = 50\Omega, and\ R_L = 20\ k\Omega$ (For the calculation of r_o, let V_A = 100 V) (10 Marks)

Question 3 **(20 Marks)**

Figure 3 shows a discrete MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. Drive and determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5\ V, k_n'\ (W/L) = 0.25\ mA/V^2$, and $V_A = 50\ V$. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

Question 4 **(10 Marks)**

A. Given figure 4, find difference mode gain Ad, common mode gain Ac, and common mode rejection ratio CMRR (5 Marks)

B. Given figure 5, show that the transfer function of can be written in the form $\frac{V_o}{V_i} = -\frac{R_2/R_1}{[1+(\omega 1/j\omega)][1+j(\omega/\omega 2)]}$ and find approximate expression for the transfer function if $\omega \ll \omega_1$ (5 Marks)

Good luck ..... Associate Prof. Tamer Abouelnaga

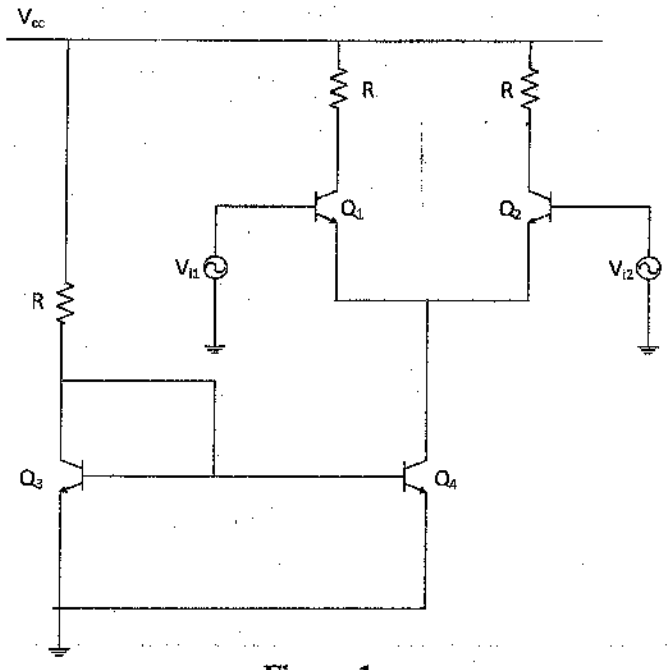

Figure 1

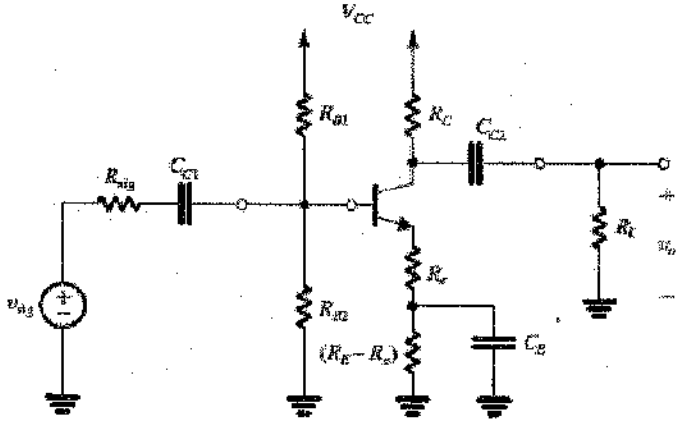

Figure 2

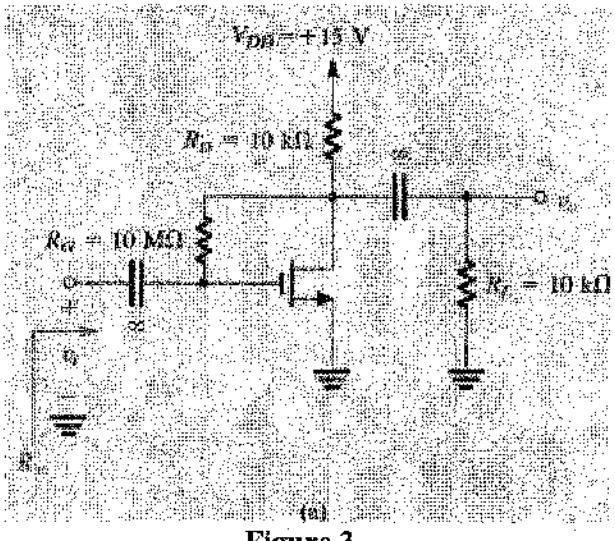

Figure 3

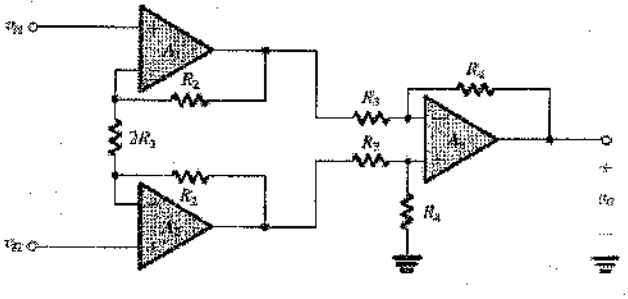

Figure 4

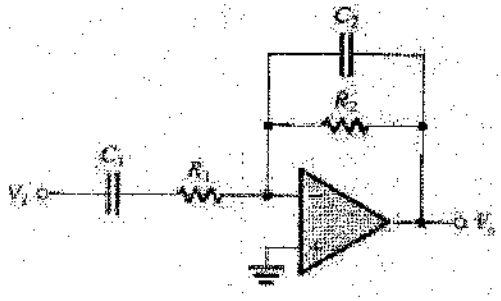

Figure 5

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Question 5 **(4 Marks)**

For the circuits shown in Fig. 6 using ideal diodes, the values of the voltages are:

a) 5 Volt or -5 Volt or 0 Volt

b) 5 Volt or -5 Volt or 0 Volt

c) 5 Volt or -5 Volt or 0 Volt

d) 5 Volt or -5 Volt or 0 Volt

Question 6 **(6 Marks)**

For the circuits shown in Fig. 7 using ideal diodes, the values of the voltages are:

a) 1 Volt or 2 Volt or -5 Volt

b) 1 Volt or 2 Volt or 5 Volt

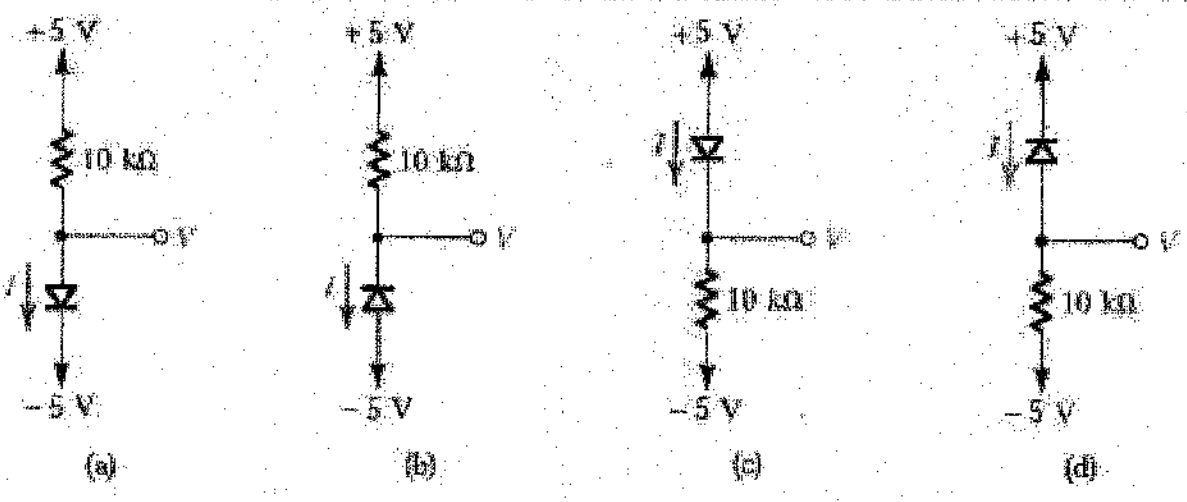

Figure 6

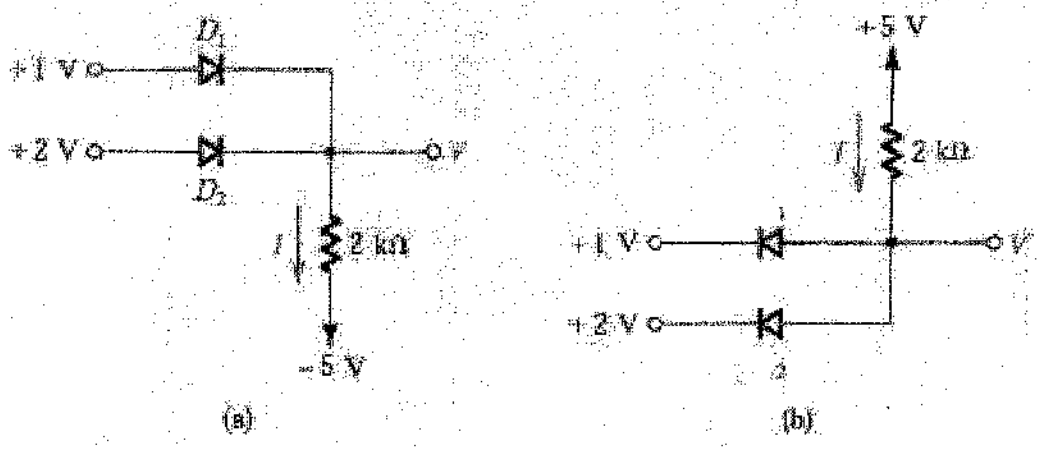

Figure 7

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