KafrelSheikh University
Faculty of Engineering
Electrical Engineering Department
Final Exam, 2019 -2020
Computer Architecture.

3th Year (Computer Engineering & systems)
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Time: 3 Hours., Mark: 60
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Dr. Wessam M. Fikry

Answer all the following questions:

This exam measures ILOs no: a3, a4, a8, a13, a14, b4, b5, b6, b13, c3, c6, c14, d1, d4

Question #1: Answer briefly on the following questions [10 marks]

1. List and briefly define the main structural components of a computer.
2. What, in general terms, is the distinction between computer organization and computer architecture?
3. What is the difference between RISC and CISC? Give example for each one, draw the architecture for each one.
4. Discuss in briefly, the types of ROM.
5. What are the modes of I/O transfer data? Discuss

Question #2- Choose the correct answer: [10 Marks]

1. Data hazards occur when.....

A. Greater performance loss. B. Pipeline changes the order of read/write access to operands.

C. Some functional unit is not fully pipelined. D. Machine size is limited.

2. Floating point representation is used to store

A. Boolean values B. whole numbers C. real numbers D. integers

3. In double precision format, the size of the mantissa is _____

A. 32 bit B. 52 bit C. 64 bit. D. 72 bit

4. Register *$2* written by subtraction can be written in instruction

A. sub $4, $1,$3 B. add $2, $1,$3 C. sub $2, $1,$3 D. mul $2, $1,$3

5- Make a decision based on results of above instruction while its being executed, is referred to as

A. Structural hazards B. Data hazards C. Control hazard D. Pipelining

6. Cache memory refers to:

A. cheap memory that can be plugged into the mother board to expand main memory
B. fast memory present on the processor chip that is used to store recently accessed data
C. a reserved portion of main memory used to save important data
D. a special area of memory on the chip that is used to save frequently used constants

7- The sign followed by the string of digits is called as _____

A. Significant B. Determinant C. Mantissa D. Exponent

8. _____ are the different type/s of generating control signals.

A. Micro-programmed B. Hardwired

C. Micro-instruction D. Both Micro-programmed and Hardwired

9. A special request originated from some device to the CPU to acquire some of its time is called _____

A. Disturbance B. Attenuation C. Interrupt D. Noise

10. An interface that provides a method for transferring binary information between internal storage and external devices is called

A. I/O interface B. Input interface C. Output interface D. I/O bus

Question #3- Answer by explanations the following questions [40 Marks]

1- Use the Booth algorithm to multiply 14 (01110) (multiplicand) by -5 (11011) (Multiplier), where each number is represented using 5 bits. [6]

2- Consider the following values, using the IEEE 754 single precision floating-point format. What is the equivalent value as a decimal number? **0 101 1100 1 010 0100 0100 0000 0000 0000** [5]

3- Show the IEEE 754 binary representation for the following floating-point numbers in single precision **-11.5** [5]

4- **If** x = 1 011 1011 1 100 1000 0000 0000 0000 0000
y = 0 100 0100 1 001 0100 1000 0000 0000 0000
With these single precision IEEE 754 floating- point numbers, perform, **x+y** [6]

5- Design a **3-bit binary** ALU operations due to the following truth table of the control signals. [6]

S_1	S_0	Operation
0	**0**	A AND B
0	**1**	A OR B
1	**0**	A XOR B
1	**1**	NOT A

6- Consider the following sequence of instructions being processed on the pipelined 5-stage. **Is there a hazard, why does it occur, and how can it be fixed Using the pipeline stalls** [6]

```
Add  $1,0($0)
Sub  $4,$1,$5
and  $6,$1,$7
or   $8,$1,$9
xor  $4, $1,$5
```

7- MIPS is a 5-stage pipelined implementation of MIPS without forwarding. Consider the following piece of code containing data hazards. **Rewrite this code so that it does the same thing on MIPS as on regular MIPS, but runs without stalls on MIPS. A stall delays every subsequent instruction by 1 cycle.** [6]

Initial code:

```
Add  $1, $2, $3
Add  $4, $1, $3
Add  $5, $6, $3
Add  $7, $8, $3
```

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