KAFR-ELSHIEKH UNIVERSITY
FACULTY OF ENGINEERING
TIME ALLOWED: 3 HOURS
DATE: 15 JANUARY 2020

ELECTRICAL ENGINEERING DEPARTMENT
COMPUTER ENGINEERING AND SYSTEMS BRANCH
1ST YEAR FINAL EXAM OF 1ST SEMESTER 2019 - 2020
LOGIC CIRCUITS [CODE NO. ECS 1004]

The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

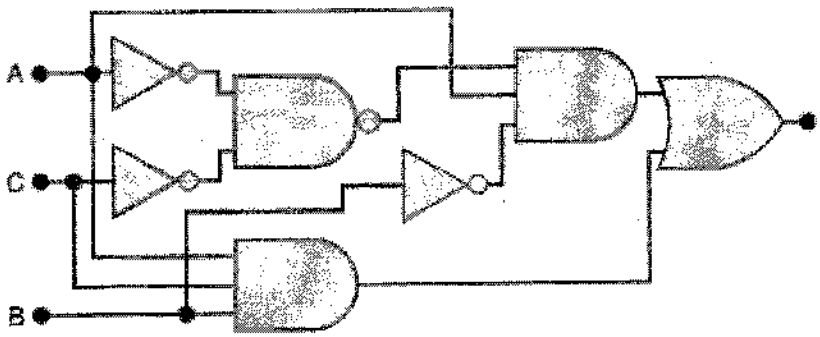
- Clarify your answer with the suitable sketches as you can.
- Please use a pen or heavy pencil to ensure legibility.
- Please attempt all questions.

QUESTION NUMBER ONE [35 MARKS]

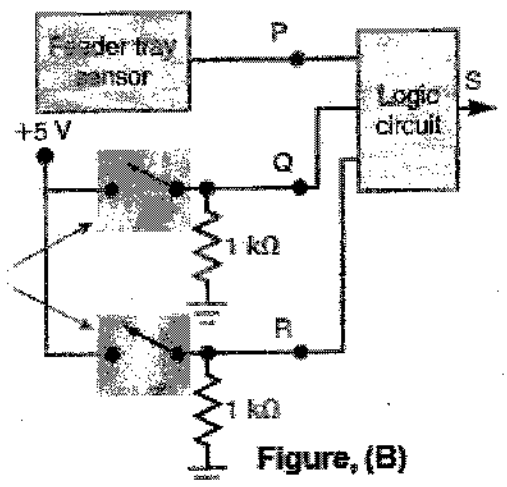
1. If M=432 and N=357, perform the signed BCD subtraction on the given unsigned decimal numbers. Afterward, draw a flow chart that corresponds to the division process. Henceforth, show the step by step multiplication process using Booth algorithm when the multiplicand is -6 and the multiplier is 2. [8 Marks]

2. For the circuit shown in figure (A), write down a logic expression for the output Z as a function of the inputs A, B and C and then use Boolean algebra to express Z in a simplified form. Hereafter, simplify the following expressions using Boolean postulates.

$$\overline{X\bar{Y} + XYZ + X(Y + X\bar{Y})}$$ [10 Marks]



Figure, (A)



Figure, (B)

3. Refer to Figure (B). In a simple copy machine, a stop signal, S is to be generated to stop the machine operation and energize an indicator light whenever either of the following conditions exists: 1) there is no paper in the paper feeder tray; or 2) the two micro-switches in the paper path are activated, indicating a jam in the paper path. Design the logic circuit to produce a **HIGH** at output signal S for the stated conditions, and then implement it using the two-input **NAND** chips. [7 Marks]

4. Design a BCD adder/subtractor using a 4-bit binary adder chip and the least number of logic gates. The adder/subtractor should receive two 4-bit numbers A and B and should produce 4-bit sum/difference and a carry/borrow output. [10 Marks]

QUESTION NUMBER TWO [25 MARKS]

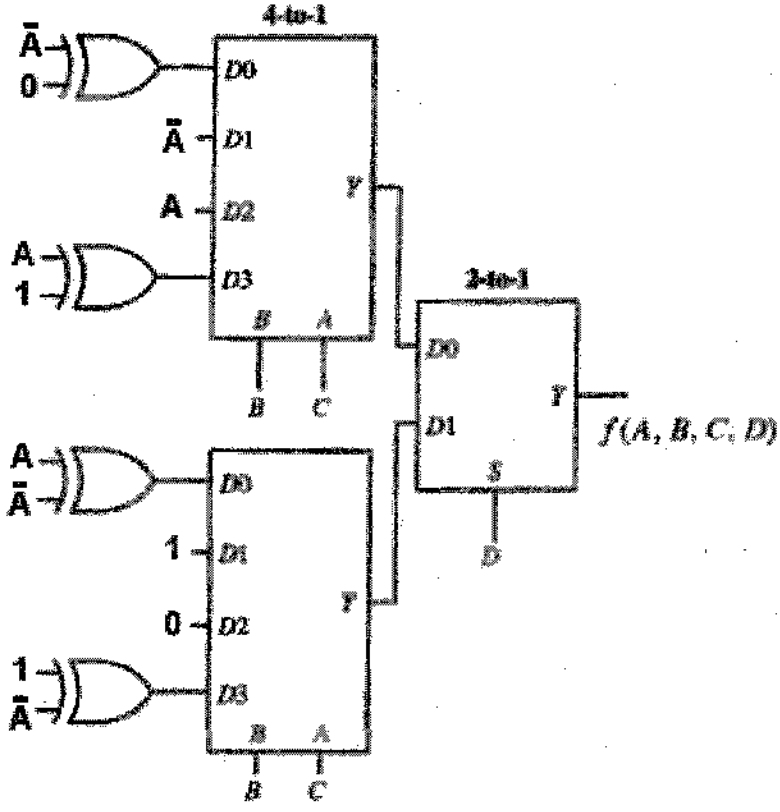
1. We have a decoder with three inputs A, B, C and eight active high outputs. In addition, there is an active law enable input "En". We wish to implement the following function using the decoder and as few NAND gates as possible. Show a block diagram. [6 Marks]

$$F(A,B,C,E) = \Sigma(1,3,7,9,15)$$

2. Implement the two-input NAND and two-input NOR functions using a single 2-to-4 decoder and a minimal number of additional OR gates. [4 Marks]

3. Find the minterm list of the function F (A, B, C, D) realized by the following figure. After that, design an 8 to 1 multiplexer by using the four variable function given by: [8 Marks]

$$F(A,B,C,D) = \Sigma\, m\,(0,1,3,4,8,9,15)$$



4. Design a combinational circuit with three inputs, X, Y and Z and three outputs, A, B and C. When the binary input is 0, 1, 2, or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6, or, 7, the binary output is three less than the input. [7 Marks]