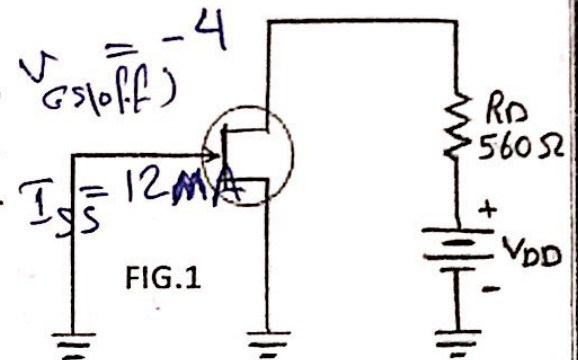




**[1] Question One[20]:**

1. Compare between voltage controlled and current controlled devices, then which of them has more gain and why.
2. Explain the structure of insulated gate FET "IGFET" and its operation.
3. For the JFET in Figure1:

a) Determine the minimum value of  $V_{DD}$  required to put the device in the constant-current region of operation when  $V_{GS} = 0$  V, If  $V_{DD}$  is increased to 15 V, what is the drain current?



b) If  $I_{DSS} = 3.0$  mA,  $V_{GS(off)} = -6$  V maximum, and  $g_{fs(max)} = 5000$   $\mu$ S. Using these values, determine the forward transconductance for  $V_{GS} = -4$  V, and find  $I_D$  at this point.

4. Design an emitter-stabilized network at  $I_{CQ} = 1/3 I_{Csat}$  and  $V_{CEQ} = 1/3 V_{CC}$ . Use  $V_{CC} = 20$  V,  $I_{Csat} = 10$  mA,  $\beta = 120$ , and  $R_C = 4R_E$ . Use standard values as possible.

**[2] Question Two[25]:**

1. How is a BJT biased for stability and how stabilized the voltage gain?
2. Prove that in a transistor operating in CE-configuration, the active region, collector current  $I_C$  is given by  $I_C = \beta I_B + (\beta + 1) I_{CBO}$

3. Modify the schematic to show how you would "swamp out" the temperature effects of  $r_e$  in Figure 2 by making  $R_e$  at least ten times larger than  $r_e$ . Keep the same total  $R_E$ . How does this affect the voltage gain?

4. Describe the operation of a transistor amplifier in CE configuration.

5. For the amplifier in Figure 3:

(a) Determine the dc collector voltage.

(b) Determine the ac collector voltage.

(c) Draw the total collector voltage waveform and the total output voltage waveform.

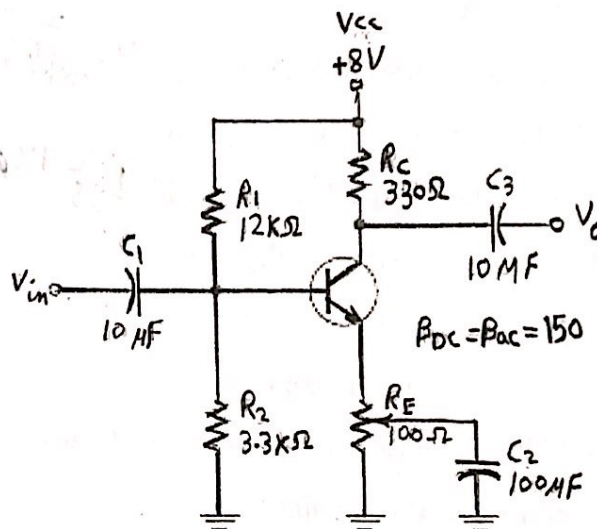
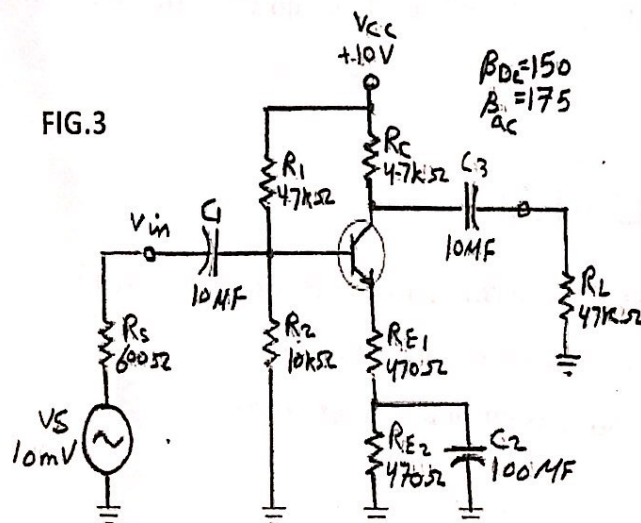


FIG. 2



$$R_{E1} = R_{E2} = 470\Omega \quad \& R_1 = R_L = 47k\Omega \quad \& R_C = 4.7k\Omega \quad \& R_2 = 10k\Omega$$

With best wishes

Dr. Noha abd-al salam

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