KAFR-ELSHIEKH UNIVERSITY
FACULTY OF ENGINEERING
TIME ALLOWED: 3 HOURS

ELECTRICAL ENGINEERING DEPARTMENT
COMPUTER ENGINEERING AND SYSTEMS BRANCH
2ND YEAR FINAL EXAM OF 2ND SEMESTER 2016 - 2017
MICROPROCESSOR SYSTEMS [CODE NO. ECS 2006]

The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

- Clarify your answer with the suitable sketches as you can.
- Please use a pen or heavy pencil to ensure legibility.
- Please attempt all questions.

QUESTION NUMBER ONE [20 MARKS]

1. Describe the different categories of instructions available in the instruction set of the basic computer. Then, draw the block diagram of a hardwired control organization with two decoders, a sequence counter and a number of control logic gates? [4 Marks]
2. Explain the various phases of instruction cycle. The following control inputs are active in the bus system of a basic computer. For each case, specify the register transfer that will be executed during the next clock transition. [3 Marks]

	S_2	S_1	S_0	LD of register	Memory	Adder
a.	1	1	1	IR	Read	-----
b.	1	1	0	PC	-----	-----
c.	1	0	0	DR	Write	-----
d.	0	0	0	AC	-----	Add

3. With a suitable diagram explain how BSA instruction is used with a subroutine. The BSA instruction is assumed to be in memory at address 20. The I-bit is 0 and the address part of the instruction has the binary equivalent 135. [3 Marks]
4. The content of PC in the basic computer is 3AF. The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F.
   1) What is the instruction that will be fetched and executed next?
   2) Show the binary operation that will be performed in the AC when the instruction is executed.
   3) Give the contents of registers PC, AR, DR, AC, and IR in hexadecimal and the values of E, I, and the sequence counter SC in binary at the end of the instruction cycle. [4 Marks]
5. Derive the Boolean expression for the gate structure that clears the sequence counter to 0. Draw the logic diagram of the gates and show how the output is connected to the INR and CLR inputs of SC. Minimize the number of gates. [6 Marks]

QUESTION NUMBER TWO [20 MARKS]

1. Write down with proper diagrams an explanatory notes on the different ways in which ROM family can be programmed. After that, explain how a 16 bit memory address is forced into eight address inputs. [7 Marks]
2. What is the purpose of $\overline{\text{BHE}}$ and A_0 pins on the 8086 microprocessor. With neat diagram indicate how a simple NAND gate decoder is used to select a 2716 EPROM (2K X 8) memory component for memory locations FF800H-FFFFFH. [6 Marks]
3. Explain with an appropriate circuit diagram, the connections require interfacing 8 chips 2732 EPROM of (4K X 8), to have the starting address located at F8000H [Hint: use suitable decoder and the necessity gates for addressing decoding]. Then, explain how will you replace the decoder in this circuit with one 82S147 PROM decoder without changing the memory size or the memory addresses? [7 Marks]

QUESTION NUMBER THREE [20 MARKS]

1. What is maskable and non-maskable interrupt? The NMI interrupt input automatically vectors through which vector type number? Give an example of non-maskable interrupt in 8085 microprocessor. A certain application requires a one-shot with a pulse width of approximately 100 ms. Show the component values. [6 Marks]
2. Explain the purpose of the trap flag (TF). Then, explain how is TF cleared and set? [5 Marks]
3. Where is interrupt descriptor table located for protected mode operation? Each protected mode interrupt descriptor contains what information? [3 Marks]
4. Explain the following instructions with example and their effect on flag.
   (i) CWD (ii) AAS (iii) BOUND [3 Marks]
5. Mention how do the following instructions differ in their functionality-
   (i) NEG & NOT (ii) DIV & IDIV (iii) AND & TEST [3 Marks]