



The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

- ⊗ Clarify your answer with the suitable sketches as you can.
- ⊗ Please use a pen or heavy pencil to ensure legibility.
- ⊗ Please attempt all questions.

### QUESTION NUMBER ONE [15 MARKS]

1. Explain what the SBB [DI - 4], DX accomplishes. If AL = F3, BH = 72 and DH = FF, list the contents of each register and the contents of each flags after the following tasks:
  - a) XADD BH, DH
  - b) CMPXCHG BH, DH[4 Marks]
2. Select the correct instruction to perform each of the following tasks:
  - a) Shift DI three places, with zeros moved into the leftmost bit;
  - b) Invert the leftmost 10 bits of the BX register without changing the rightmost 6 bits.
  - c) Move the DH register right one place, making sure that the sign of the result is the same as the sign of the original number[5 Marks]
3. What is done with the remainder after a division? Afterward, write a short sequence of instructions that divides the number in AX by the number in BL and then round the unsigned result. Then, write a short sequence of instructions that divides the number in BL by the number in CL and then multiplies the result by 2. The final answer must be a 16-bit number stored in the DX register. [6 Marks]

### QUESTION NUMBER TWO [15 MARKS]

1. Contrast the operation of JMP [DI] with JMP FAR PTR [DI]. Which type of JMP instruction (short, near, or far) assembles for the following:
  - a) If the distance is 0210H bytes
  - b) If the distance is 0020H bytes
  - c) If the distance is 10000H bytes[5 Marks]
2. Write a complete assembly program that uses while loop to read data from the keyboard and store it into an extra memory segment array called BUF until CR key "OD<sub>H</sub>" is typed. [5 Marks]
3. Explain the purpose of the trap flag. Write a procedure that clears the TF to disable trapping. [5 Marks]

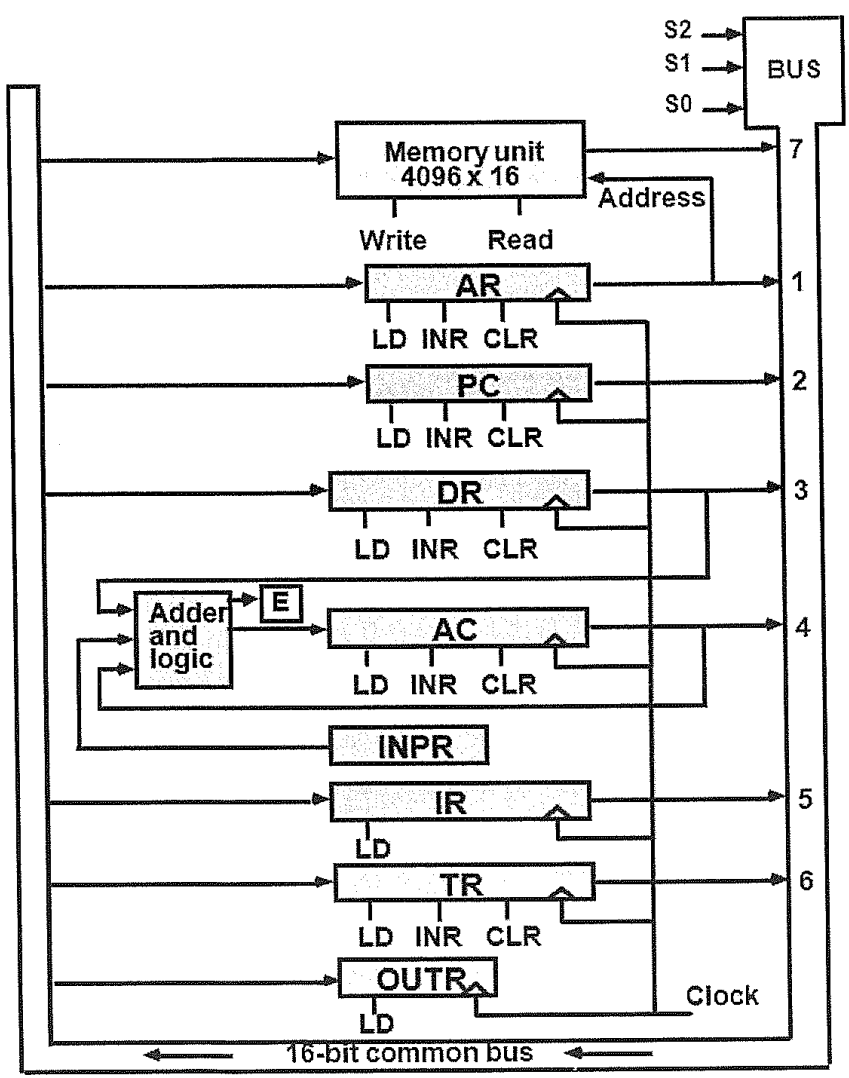
### QUESTION NUMBER THREE [15 MARKS]

1. Where are the interrupt vectors located in the microprocessor's memory? Then describe the differences between a protected and real mode interrupt. After that, list the events that occur when an interrupt becomes active. [4 Marks]
2. When a hardware interrupt occurs, how does the microprocessor determine the interrupt vector type number? In your explanation, I expect to see a circuit diagram that applies any interrupt vector type number in response to INTA pin. [6 Marks]
3. Explain the operation of the IRET. When will the BOUND instruction interrupt a program? What is the purpose of interrupt vector type number 3? [5 Marks]

### QUESTION NUMBER FOUR [15 MARKS]

1. Show the contents in hexadecimal of registers PC, AR, DR, IR, and SC of the basic computer when an ISZ indirect instruction is fetched from memory and executed. The initial content of PC is 7FF. The content of memory at address 7FF is EA9F. The content of memory at address A9F is 0C35. The content of memory at address C35 is FFFF. Give the answer in a table with five columns, one for each register and a row for each timing signal. Show the contents of the registers after the positive transition of each clock pulse. [5 Marks]
2. Show the gate structure associated with the control inputs of AR. In similar fashion derive the control gates for the read & write inputs of the memory in the basic computer. [5 Marks]
3. The following register transfers are to be executed in basic computer. For each transfer, Specify:
  - A. The binary value that must be applied to bus select inputs S2, S1, and S0;
  - B. The register whose LD control input must be activate (if any);
  - C. A memory read or write operation (if needed); and
  - D. The operation in the adder and logic circuit (if any).
  1.  $AR \leftarrow PC$
  2.  $IR \leftarrow M[AR]$
  3.  $M[AR] \leftarrow TR$
  4.  $AC \leftarrow AC + DR$[3 Marks]
4. Derive the Boolean expression for X2. [2 Marks]

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Fetch R'T0: AR ← PC  
 R'T1: IR ← M[AR], PC ← PC + 1  
 Decode R'T2: D0, ..., D7 ← Decode IR(12 ~ 14), AR ← IR(0 ~ 11), I ← IR(15)

Indirect D7'IT3: AR ← M[AR]

Interrupt: R ← 1  
 RT0: AR ← 0, TR ← PC  
 RT1: M[AR] ← TR, PC ← 0  
 RT2: PC ← PC + 1, IEN ← 0, R ← 0, SC ← 0

Memory-Reference:

AND D0T4: DR ← M[AR]  
 D0T5: AC ← AC . DR, SC ← 0  
 ADD D1T4: DR ← M[AR]  
 D1T5: AC ← AC + DR, E ← Cout, SC ← 0  
 LDA D2T4: DR ← M[AR]  
 D2T5: AC ← DR, SC ← 0  
 STA D3T4: M[AR] ← AC, SC ← 0  
 BUN D4T4: PC ← AR, SC ← 0  
 BSA D5T4: M[AR] ← PC, AR ← AR + 1  
 D5T5: PC ← AR, SC ← 0  
 ISZ D6T4: DR ← M[AR]  
 D6T5: DR ← DR + 1  
 D6T6: M[AR] ← DR, if(DR=0) then (PC ← PC + 1), SC ← 0

Register-Reference:

D7'IT3 = r (Common to all register-reference instructions)  
 IR(i) = Bi (i = 0,1,2, ..., 11)  
 r: SC ← 0  
 CLA rB11: AC ← 0  
 CLE rB10: E ← 0  
 CMA rB9: AC ← AC'  
 CME rB8: E ← E'  
 CIR rB7: AC ← shr AC, AC(15) ← E, E ← AC(0)  
 CIL rB6: AC ← shl AC, AC(0) ← E, E ← AC(15)  
 INC rB5: AC ← AC + 1  
 SPA rB4: If(AC(15)=0) then (PC ← PC + 1)  
 SNA rB3: If(AC(15)=1) then (PC ← PC + 1)  
 SZ rB2: If(AC = 0) then (PC ← PC + 1)  
 SZE rB1: If(E=0) then (PC ← PC + 1)  
 HLT rB0: S ← 0

Input-Output:

D7'IT3 = p (Common to all input-output instructions)  
 IR(i) = Bi (i = 6,7,8,9,10,11)  
 p: SC ← 0  
 INP pB11: AC(0-7) ← INPR, FGI ← 0  
 OUT pB10: OUTR ← AC(0-7), FGO ← 0  
 SKI pB9: If(FGI=1) then (PC ← PC + 1)  
 SKO pB8: If(FGO=1) then (PC ← PC + 1)  
 ION pB7: IEN ← 1  
 IOF pB6: IEN ← 0