KAFRELSHEIKH UNIVERSITY
FACULTY OF ENGINEERING
TIME ALLOWED: 3 HOURS

ELECTRICAL ENGINEERING DEPT. 2nd YEAR
FINAL EXAM OF 1ST SEMESTER 2015-2016
MICROPROCESSOR SYSTEMS

The maximum mark for the examination paper is 60 marks, and the mark obtainable for each part of a question is shown in brackets alongside the question.

Instructions to the candidates:

- Clarify your answer with the suitable sketches as you can.
- Please use a pen or heavy pencil to ensure legibility.
- Assume any missed data reasonably.
- Please attempt all questions.

QUESTION NUMBER ONE [25 MARKS]

1. What does the term "memory access time" mean? Why does instruction that requiring memory access takes machine cycles more than instruction that requiring register access? [4 Marks]
2. What is the purpose of the system buses? Which bus controls how much memory you can have? Which control signal causes the memory to perform a read operation? Does the size of the data bus control the maximum value the CPU can process? Explain. [5 Marks]
3. Show how the flag register is affected by the addition of E023 and ABOF. Will an overflow occur if a signed FF is added to a signed 01? Which instructions set and clear the D-flag? [5 Marks]
4. Describe what happens when a new number is loaded into a segment register when microprocessor is operated in the protected mode? In the real mode, show the starting and ending addresses of each segment located by the following segment register value: AB00H. [4 Marks]
5. Code a descriptor that describes a memory segment that begins at location 03000000H and ends at location 05FFFFFFH. This memory segment is a data segment that grows upward in the memory system and can be written. The descriptor is for a Pentium 4 microprocessor. [5 Marks]
6. What assembly language directive indicates the start of the code segment? What is the purpose of the .MODEL TINY statement? What tasks does the .data directive accomplished in the small memory model? [2 Marks]

QUESTION NUMBER TWO [25 MARKS]

1. What, if anything, is wrong with a MOV AL, [BX] [SI]? What is a displacement? How does it determine the memory address in a MOV DS: [2000H], AL instruction? [4 Marks]
2. Explain the difference between the MOV BX, DATA instruction and the MOV BX, OFFSET DATA. [5 Marks]
3. Suppose that DS = 1000H, BX = FF00H, and DI = 1000H. Determine the memory address accessed by the following instruction, assuming real mode operation: MOV AL, [BX+DI] [3 Marks]
4. Which instruction places the EFLAGS on the stack in the Pentium 4 microprocessor? What segment register may not be popped from the stack? Then, explain what happens when the PUSH BX instruction executes. Make sure to show where BH and BL are stored (Assume that SP = 0100H and SS = 0200H.) [6 Marks]
5. In a machine language instruction, what information is specified by the MOD field? Convert an 8B9E004CH from machine language to assembly language. If a MOV SI, [BX+2] instruction appears in a program, what is its machine language equivalent? [7 Marks]

Turn the page to see the rest of the questions

QUESTION NUMBER THREE [10 MARKS]

1. Describe how the LDS BX, NUMB instruction operates. [2 Marks]
2. Explain the operation of the LODSQ instruction for the 64-bit mode of the Pentium 4 or Core2. Then, explain the operation of the OUTSB instruction. [4 Marks]
3. Write a short sequence that read data from extra segment memory location 046CH and stored it an array that is indirectly addressed through register BX (containing 50 bytes). [4 Marks]

Given the contents of the microprocessor 80286

(IP) = 032FH	(BX) = 1200H	(AX) = A1B2H	Disp = 3100H
(CS) = 1000H	(DS) = 2000H	(CX) = D7E6H	(BP) = 1000H
(ES) = 3000H	(SS) = 2000H	(DX) = E1C2H	(SP) = 15FCH

32-bit mode selected R/M

R/M Code	*Function*
000	DS:[EAX]
001	DS:[ECX]
010	DS:[EDX]
011	DS:[EBX]
100	Uses scaled-index byte
101	SS:[EBP]*
110	DS:[ESI]
111	DS:[EDI]

**Note:* See text section, Special Addressing Mode.

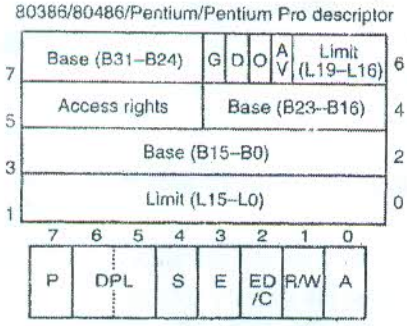
The scaled-index byte.

SS
00 = × 1
01 = × 2
10 = × 4
11 = × 8

Segment register Selection

Code	*Segment Register*
000	ES
001	CS*
010	SS
011	DS
100	FS
101	GS

80386/80486/Pentium/Pentium Pro descriptor



REG and R/M when MOD = 11

Code	*W=0 (Byte)*	*W=1 (Word)*	*W=1 (Doubleword)*
000	AL	AX	EAX
001	CL	CX	ECX
010	DL	DX	EDX
011	BL	BX	EBX
100	AH	SP	ESP
101	CH	BP	EBP
110	DH	SI	ESI
111	BH	DI	EDI

16bit R/M memory mode

R/M code	*Addressing Mode*
000	DS:[BX+SI]
001	DS:[BX+DI]
010	SS:[BP+SI]
011	SS:[BP+DI]
100	DS:[SI]
101	DS:[DI]
110	SS:[BP]*
111	DS:[BX]