

1-Answer briefly on the following questions[25 points]

1. What in general terms, is the distinction between computer structure and computer function?

- Structure: is the way in which components relate to each other.
- Function: is the operation of individual components as part of the structure

2. What are the four main functions of a computer?

Data processing: Computer must be able to process data which may take a wide variety of forms and the range of processing.

Data storage: Computer stores data either temporarily or permanently.

Data movement: Computer must be able to move data between itself and the outside world.

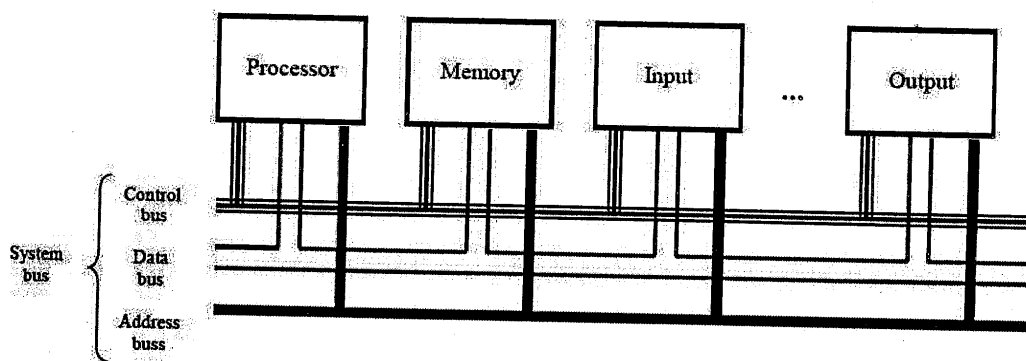
Control: There must be a control of the above three functions.

3. In relation to computer architecture, what are buses?

(i)**Address bus:**Address bus is used to carry the address. It is unidirectional bus. The address is sent to from CPU to memory and I/O port and hence unidirectional. It consists of 16, 20, 24 or more parallel signal lines.

(ii)**Data bus:**Data bus is used to carry or transfer data to and from memory and I/O ports. They are bidirectional. The processor can read on data lines from memory and I/O port and as well as it can write data to memory. It consists of 8, 16, 32 or more parallel signal lines.

(iii)**Control bus:**Control bus is used to carry control signals in order to regulate the control activities. They are bidirectional. The CPU sends control signals on the control bus to enable the outputs of addressed memory devices or port devices.



Bus interconnection scheme

4. Discuss in briefly the types of RAM.

Static RAM (SRAM)

The static RAM consists of flip flop that stores binary information and this stored information remains valid as long as power is applied to the unit.

Dynamic RAM (DRAM)

- The dynamic RAM stores the binary information in the form of electrical charges and capacitor is used for this purpose.
- Since charge stored in capacitor discharges with time, capacitor must be periodically recharged and which is also called *refreshing memory*.

5- What is a pipeline hazard? What are their types? Discuss

Pipeline hazard: Any condition that causes the pipeline to stall is called hazard. They are also called as stalls or bubbles.

The types of pipeline hazards

The various pipeline hazards are:

- (i) Data hazard, (ii) Structural Hazard, and (iii) Control Hazard.

Data hazard

Any condition in which either the source or the destination operand of an instruction are not available at the time expected in the pipeline is called data hazard.

Instruction or control hazard

The pipeline may be stalled because of a delay in the availability of an instruction. For example, this may be a result of a miss in the cache, requiring the instruction to be fetched from the main memory. Such hazards are often called control hazards or instruction hazard.

Structural hazards.

This is the situation when two instruction require the use of a given hardware resource at the same time. The most common case in which this hazard may arise is in access to memory.

6. What are the modes of I/O transfer data?

Programmed I/O

Interrupt Driven I/O

Direct Memory Access (DMA)

7- Describe the function of the following in the fetch-execute cycle.

- Program counter
- The address bus
- The data bus
- The decoder
- The Arithmetic and Logic unit

- Program counter:

This is a register in the CPU which contains the memory address of the next instruction to be processed.

- The address bus:

The memory address of the instruction to be fetched is transmitted from the program counter to the RAM through the address bus.

- The data bus:

The data is transmitted from RAM back to the instruction register in the CPU through the data bus.

- The decoder:

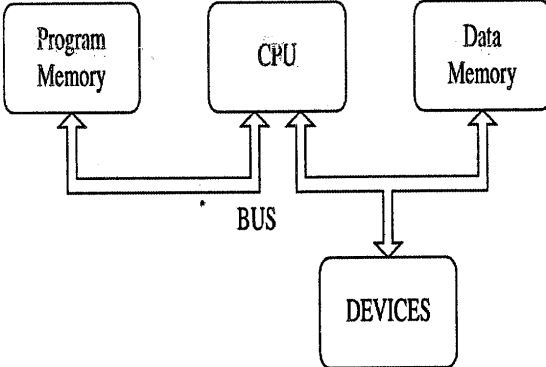
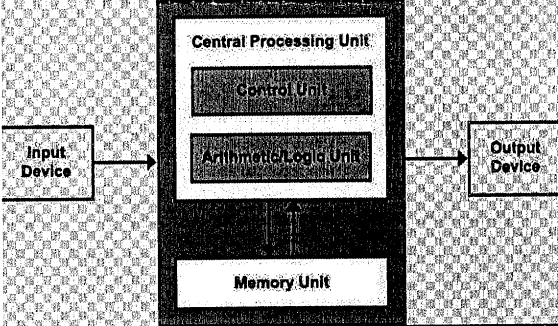
The decoder in the control unit works out what the instruction means – what has to be done to the data.

- The Arithmetic and Logic unit:

Perform mathematical operations such as addition, subtraction, multiplication and division. Additionally, the ALU processes basic logical operations like AND/OR calculations.

2- Discuss with illustration by drawing [5 points]

1- Distinguish between Von-Neumann Architecture and Harvard Architecture

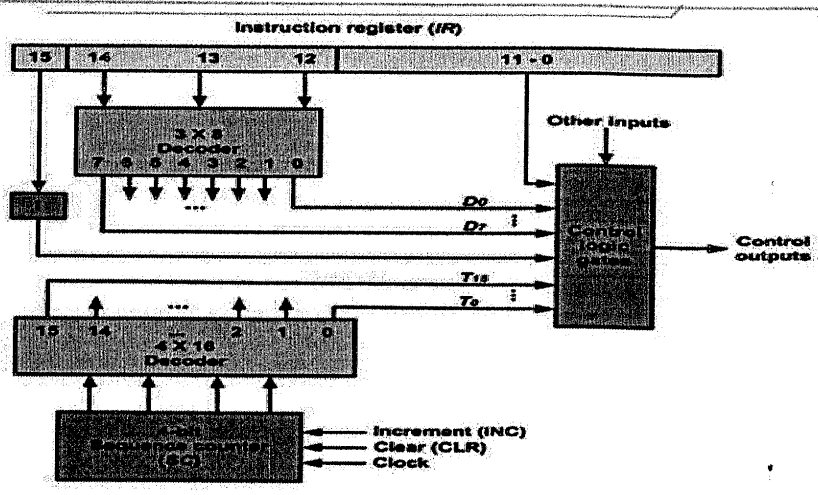
Harvard	Von-Neumann
<ul style="list-style-type: none"> - Two memories with two Buses allow parallel access to data access and instructions. - Control unit for two buses is more complicated and more expensive. - Program cannot write itself. - Both memories can use different sizes. - Development of a complicated Control Unit needs more time. - Free data memory can't be used for instruction and vice-versa. 	<ul style="list-style-type: none"> - Content of the memory if organized and all installed memory can be used. - One bus is simpler for the control unit design - Computer with one bus is cheaper. - Error in a program can rewrite instruction and crash program execution. - Development of the Control Unit is cheaper and faster. - Data and instruction is accessed in the same way. - One Bus (for Data, instruction and devices) is a bottleneck.
 <p>The diagram illustrates the Harvard architecture. It features three boxes at the top: 'Program Memory', 'CPU', and 'Data Memory'. Below them is a box labeled 'DEVICES'. A central horizontal line represents the 'BUS'. Arrows point from the 'BUS' to each of the three top boxes. A vertical line descends from the 'BUS' to the 'DEVICES' box, with an arrow pointing downwards.</p>	 <p>The diagram illustrates the Von-Neumann architecture. It shows a central vertical stack of components: 'Central Processing Unit' (containing 'Control Unit' and 'Arithmetic Logic Unit') and 'Memory Unit' below it. To the left is an 'Input Device' with an arrow pointing to the 'Central Processing Unit'. To the right is an 'Output Device' with an arrow pointing from the 'Central Processing Unit'. The 'Memory Unit' is connected to the 'Arithmetic Logic Unit'.</p>

2- The components the Control unit of a basic computer.

Control unit of a basic computer [slide 18]

Consists of:

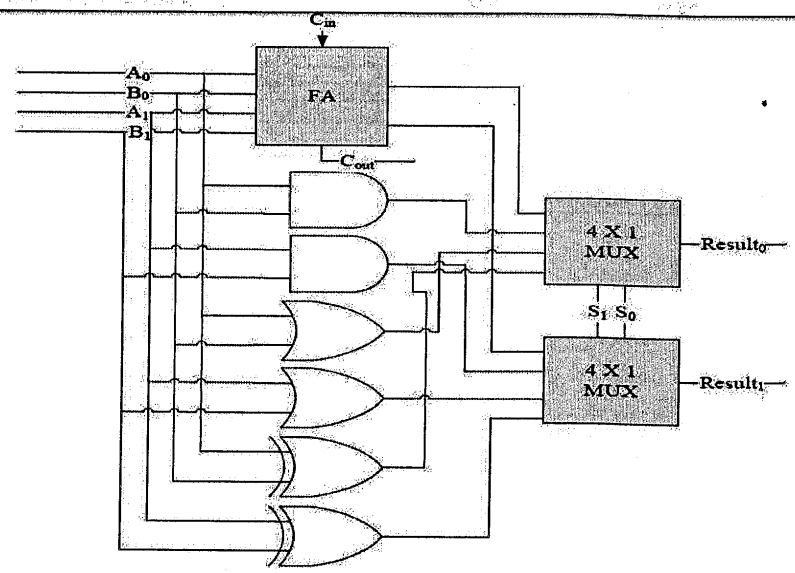
- 1- Opcode Decoder 3X8 [D0 – D7]
- 2- Timing Decoder 4X16 [T0 – T15]
- 3- 4-bit sequence counter
- 4- Control logic gates
- 5- IR register with 16-bit



3- Answer by explanations the following questions [25 points]

1- Design a 2-bit binary ALU operations due to the following truth table of the control signals.

S1	S2	operation
0	0	A OR B
0	1	A AND B
1	0	A XOR B
1	1	A + B



2- Multiply given signed 2'S complement numbers
 A = 110101 multiplicand (-11) B = 011011 multiplier (+27)

3-(2) Midterm Answer (-11) $A = 110101$ M
 $B = 011011$ Q
 A Q Q' M $\bar{M}+1$ Count operation

000000 011011 0 110101 001011 6
 001011
 001011
 001011 011011 1 $A \leftarrow A - M$
 shift right

000010 110101 1 5
 shift right

110101 4
 110111 110101 1 $A \leftarrow A + M$
 111011 111011 0 shift right

001011 3
 000110 111011 0 $A \leftarrow A - M$
 000111 011011 1 shift R

000001 101101 1 2
 shift R

110101 1
 110110 101101 1 $A \leftarrow A + M$
 111011 010111 0 shift R

0
 result A Q
 111011 010111 $-2^8 + 2^9 + 2^7 + 2^6 + 2^4 + 2^3 + 2^2 + 2^1 = -297$

3- Consider 4-bit dividend and 2-bit divisor:
 Dividend = 1010 Divisor = 0011

(3)

3. Division 4-bit Dividend = 1010 = Q
 Divisor = 0011 = M M+1 = 1101

A	Q	Count	
0000	1010	4	
0001	0100		Shift left
1101			A ← A - M
0110			Q ₀ ← 0
0011			A ← A + M
0001	0100		
0001	0100	3	
0010	1000		SHL
1101			A ← A - M
0111			Q ₀ ← 0
0011			
0010	1000	2	
0101	0000		SHL
1101			A ← A - M
0010	0001		Q ₀ ← 1
0100	0010	1	
1101			SHL
0001	0011		A ← A - M
0001	0011		Q ₀ ← 1
remainder A = 1	Q = 3	0	

4- Add single precision floating point numbers A and B, where
 A = 44900000H and B = 42A00000H

3- Add in Floating Point

(4) $A = 44900000H$ $B = 42A00000H$

$A = 0100\ 0100\ 1001\ 0000\ 0000\ 0000\ 0000\ 0000$
 $B = 0100\ 0010\ 1010\ 0000\ 0000\ 0000\ 0000\ 0000$

<p style="text-align: center;">A</p> <p>$S = 0$</p> <p>$e = 10001001 = 137$ <small>تعداد البتات</small></p> <p>$137 - 127 = 10$</p> <p>$A = 1.001000 \times 2^{10}$ $= 1.0010.000 \times 2^6$</p>	<p style="text-align: center;">B</p> <p>$S = 0$</p> <p>$e = 10000101 = 133$ <small>تعداد البتات</small></p> <p>$133 - 127 = 6$</p> <p>$B = 1.010000 \times 2^6$</p>
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$Z = A + B$

$$\begin{array}{r} 1.0010.0000 \times 2^6 \\ 1.0100 \times 2^6 \\ \hline 1.0011.0100 \times 2^6 \\ \hline = 1.00110100 \times 2^{10} \end{array}$$

Normalize

$10 + 127 = 137 = 10001001$

$\therefore Z = 0100010010011010000000000000$
 $449A0000H$

5- Multiply (-18.25) by (9.5) using IEEE-754 32-bit floating-point format.

3-(5)

Multiply (-18.25) by (9.5) using IEEE 754 32 bit

$$X = 9.5$$

$$Y = -18.25$$

$$10011000$$

$$= 10010.01$$

$$= 1.0011000 \times 2^3$$

$$= 1.001001 \times 2^4$$

$$3 + 127 = 130 = 1000010$$

$$4 + 127 = 131 = 1000011$$

$$X = 0100000100011000000000$$

$$Y = 1100000101000000000000$$

$$Y = 1.001001 \times 2^4$$

$$X = 1.0011 \times 2^3$$

$$1001001 \times 2^7$$

$$10010010$$

$$1001001$$

$$10101101011 \times 2^7$$

$$= 1.0101101011 \times 2^8$$

$$8 + 127 = 135 = 10000111$$

$$Z = 11000011101011010110000000$$

$$= -173.375$$