Kafrelsheikh University - Faculty of Engineering			
Course	Integrated Circuits	Date	11/3/2021
Time	3 Hours	Mark	90
Students	4th year Electronics and Electrical Communications		

This exam measures competences no.: A.1, B.2. B.3, C.1, C.3.

Answer all the following questions:

Clarify your answer with the suitable diagrams.

Q.1 Explain the following: (10 Marks)

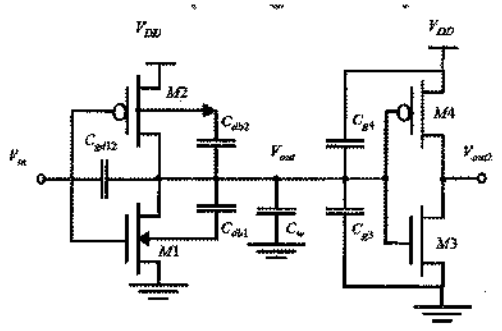
a- The parallel – plate capacitance and fringing capacitance of the wire.

b- The skin effect of the wire.

Q2.a How to evaluate the performance of a digital circuit? (5 Marks)

Q2.b Draw the Static CMOS inverter and State its properties. (5 Marks)

Q3. The following are the parasitic capacitances of Static CMOS inverter. (10 Marks)

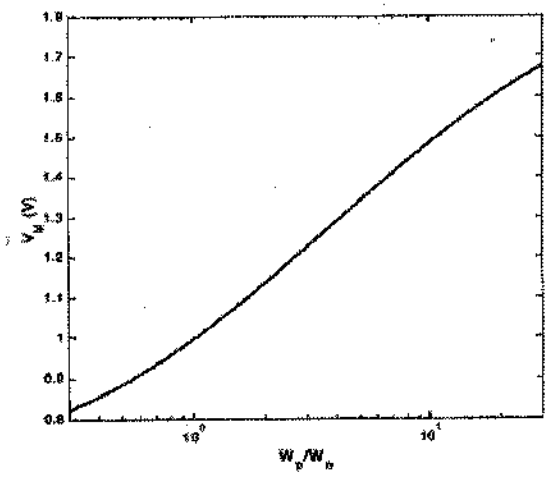


Analyse the parasitic capacitances using the Miller effect.

Q.4 a Assume a wafer size of 40 cm, a die size of 6 cm^2, 1 defects/cm^2, and $\propto = 3$. Determine the die yield of this CMOS process run. (5 Marks)

Q.4.b Prove that the Elmore delay of an RC chain equals to RC/2 . (10 Marks)

Q5.a The following curve of the simulated inverter switching threshold the Static CMOS inverter. (5 Marks)



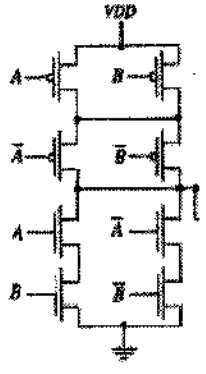
Explain and Analyze this curve to get observations about the Static CMOS inverter.

Q5.b Explain the Concept of design of the Complementary CMOS gates. (10 Marks)

Q6. Design the following CMOS gate whose function is

$$F = D + A\,(B + C)$$ (15 Marks)

Q7. Find the logic expression for the following static CMOS gate: (15 Marks)



Verify your Answer with the truth table.

Good Luck and Best Wishes ***Dr. Ibrahim Elashry***