A Novel Multistage Fuzzy Controller for FACTS Stabilization Scheme for SMIB AC System

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Abstract:- **This paper proposes a novel FACTS based Scheme controlled by a hierarchical two-stage fuzzy logic (HFLC)-multi loop dynamic error driven controller. The proposed scheme includes separate Fuzzy control stages for the PD and PID parts to ensure robust and effective dynamic speed control and efficient energy utilization. The PD fuzzy stage used the global error and change of error as the fuzzy input variables. The second stage is the PID-FLC regulation which utilizes the output of the PD-FLC stage and the integral of the global error as input fuzzy variables. The simulation results validate the proposed control scheme effectiveness and robustness with Efficient Energy Utilization, improved power quality and Power Factor at the Common AC Bus and load bus. A complete simulation model of the proposed system is developed in Matlab/Simulink/Simpower Software Environment using operational dynamic blocks available in Simulink library.**

Index Terms- **Multi-Stage Fuzzy logic controller; FACTS; Hybrid Switched Capacitive compensator-HSCC; efficient energy utilization, voltage stabilization.**

I. INTRODUCTION

THE power quality, Smart Grid Efficient Utilizations and voltage stabilization are now key operational issues. The use of static power converters in electricity has the potential for increasing the capacity of transmission line and improving the supply quality of the electric energy. Flexible AC transmission system (FACTS) devices are used in transmission control whereas custom power devices are used for distribution control. Advantage of modern control systems for switching for modulated filter schemes [1]. Combing low cost power filters with switched capacitor banks for power quality enhancement, power factor correction and energy loss reduction. This used in smart grid networks supplied by renewable energy sources [2-5]. The conventional proportional-integral-derivative (PID) type controller is the best controller used in practice. Because of its simplicity for design and its gain parameters can be tuned manually, using Ziegler-Nichols, analytical methods, Tabu search [6], particle swarm optimization [7], Genetic Algorithm [8]. pole placement method etc. A hierarchical multi-stage fuzzy logic controller has parallel and series levels where the output of one level becomes the input to the other [13-15]. Typically, pairs of inputs are fuzzified and applied to the rules of the preliminary levels. The outputs of these levels are applied to the rules of subsequent levels of the fuzzy logic system until the result of the final level gives the output of the complete fuzzy logic controller [9].This study introduces a novel Hybrid Series-Parallel Switched Capacitor Compensation (HSCC) validated for power quality and power factor enhancement with effective voltage stabilization [4]. Two types of controllers are proposed based on multi-loop dynamic error driven time-descaled and coordinated regulation scheme. The first is PID controller with fixed gains for the regulator. The second is the hierarchical Fuzzy Logic Controller that used the global error and change of error as input variables. A complete simulation model of the proposed system is developed in Matlab/Simulink/Simpower Software Environment using operational dynamic blocks available in Simulink library. This paper is organized as follows. Following introduction, The Hybrid Switched Capacitor Compensation (HSCC) scheme is given. Then the proposed Multi-Tier Fuzzy logic controller is explained. The system simulation with proposed control technique under different operating conditions are preceded the discussion of the results and conclusions.

II. THE HYBRID SERIES-PARALLEL SWITCHED CAPACITOR COMPENSATION (HSCC) SCHEME

The configuration of the proposed HSCC scheme is shown in Fig. 1.

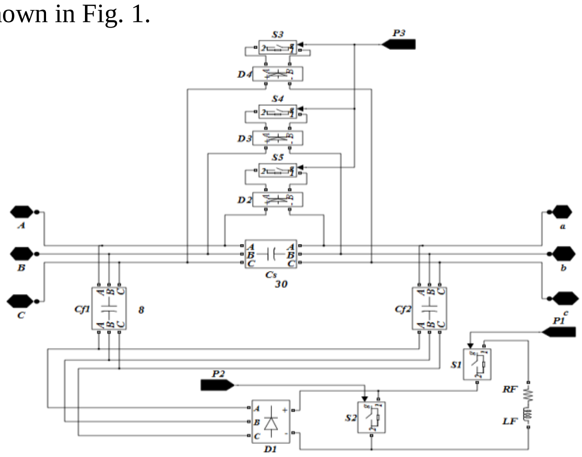

Fig 1: Hybrid Series-Parallel Switched Capacitor Compensation (HSCC) scheme Located at Feeder Mid-Point.

This device is a low cost switched/modulated filter that comprises a shunt capacitor banks connected to AC side of a three-arm uncontrolled rectifier and a series switched capacitor bank. The operational mode of FACTS is defined as follows based on the two controlled signals: Switches S2, S3, S4 and S5 are controlled by PWM pulses through P2 and P3. Whereas S1 is controlled by pulses comes from PWM through P1. These pulses are complementary and follow NOT LOGIC command, which is while P1 is on P2, is off and vice versa. It means switch S1 is operation dictates on-off state of the series capacitor bank. While other switches S2, S3, S4 and S5 are on, HSCC compensates reactive power like a shunt capacitor bank.

III. Dynamic Error Driven Control

The dynamic error driven controller and used in [10], [11] and [12]. The first dynamic tracking regulator *A* includes three loops. The first loop tracks the voltage reference whereas the second and third loops for stabilizing current excursions and limit generator power excursions, respectively. The minimal ripple content regulator *B* used to minimizes ripple in the voltage and current waveforms that used in a tri-loop error to mitigate the harmonics. Both Regulators utilizes the Multi-Tier Hierarchical Fuzzy Logic Control Scheme to ensure optimal on-off switching of pulse width modulation stages as shown in Fig. 2.

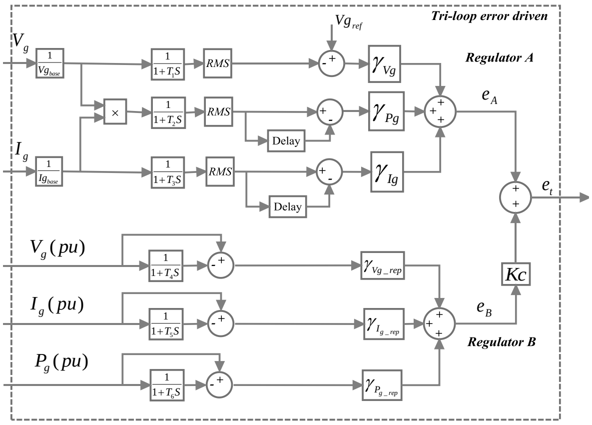

Fig 2: The Block diagram of the Tri-Loop error driven Controller.

IV. Multi-Stage Hierarchical Fuzzy Logic Control Structure (HFLC)

The structure of the Two-Stage Hierarchical Fuzzy Logic Two-Stage PID controller has the same effect and equivalent action of a PID controller as shown in Fig 3. Also, the design of the hierarchical fuzzy PID controller begins with the design of a PDFLC to give optimal results. The integral feedback is blended with the fuzzy switch to form the PIDFLC, after the PDFLC is optimized. The first step in the fuzzy controller design is selecting of the input and output variables to represent the (PDFLC). The global error; e_t and the rate of change in error ($\acute{e}_t$) are the input variables to the PDFLC. The next step PIDFLC utilized the output of the PDFLC level and the integral of the global error ($\int e$) as an input variable. Each input variables, (e_t) and ($\acute{e}_t$), for PDFLC is accompanied with a five Gaussian membership functions. The PD value represents the PDFLC output and described by a five membership functions. A full rule base, 25 rules, is also defined for PDFLC. The rules have the general form:

If e_t is *NS* and $\dot{e}_t$ is *Z* then *PD value* is *NS*.

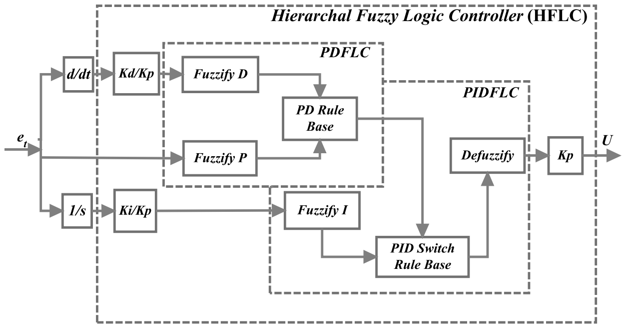

Fig 3: Two-Level Hierarchal Fuzzy Logic Controller for (HSCC FACTS) energy utilization system.

Where the membership functions (mf_i) is defined as follows: $mf_j \in \{NL, NS, Z, PS \text{ and } PL\}$ However, the output space has 25 different fuzzy sets. The PIDFLC represents the decision maker of the hierarchical fuzzy controller and its structure has two input variables PD value which is the output of PDFLC and the error integrator $\int e_t$. The PD input variable accompanied with five fuzzy set, while the second input variable, error integral, is evaluated through three fuzzy set. Therefore, the PIDFLC used a full rule base equal 15 rules. In addition, Fig. 4 and Fig. 5 show the surface rule viewers for the two controllers; PDFLC and PIDFLC respectively. So, the full rules base of the HFLC is 40 rules instead of 125 rules for the classical FLC method used three input variables.

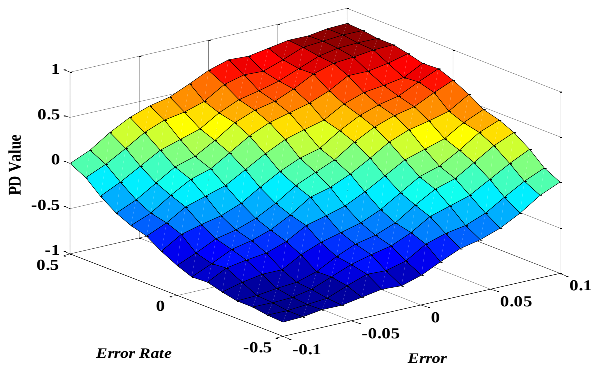

Fig 4: Rule Assignment Surface viewer of the PDFLC.

The output signal (*U*) of the Multi-Tier Hierarchical Fuzzy Logic Control Structure (HFLC) enters a PWM signal generator. On-off switching sequences produced by PWM define two operating modes of the FACTS device. The global output signal of the dynamic error driven controller is followed by a Weighted-Modified PID controller (WMPID) as in [5]. The simulation results compare between the proposed (HFLC) with WMPID controllers for FACTS.

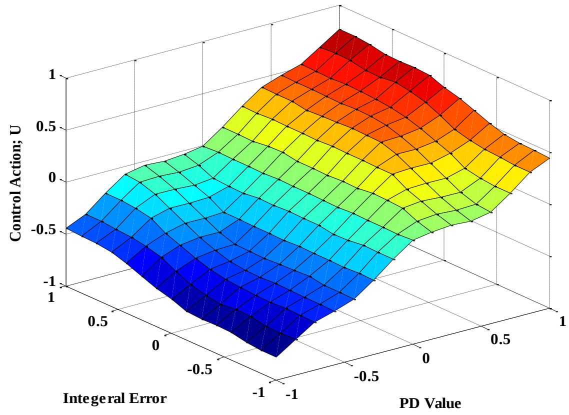

Fig 5: Rules surface viewer of the PIDFLC.

V. Digital Simulation Results and Discussions

The Unified Study AC system configuration is shown in Fig. 6. This system comprises a hybrid AC load of linear, converter type nonlinear and induction motor loads that connected to the load bus as shown in Fig. 7.

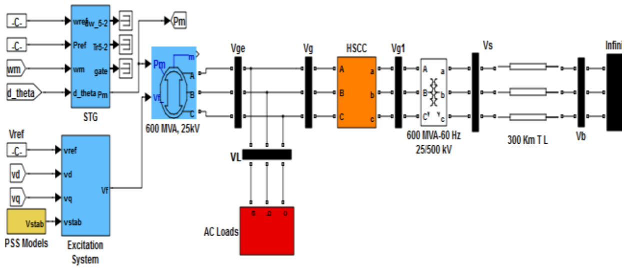

Fig 6: AC Grid with FACTS-(HSCC) scheme Located at Feeder Mid-Point.

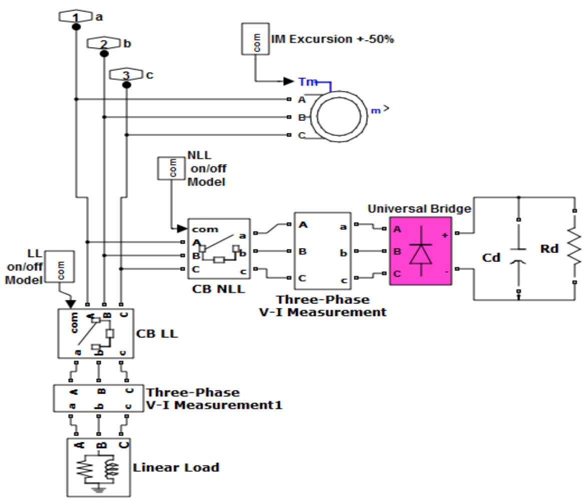

Fig 7: AC Hybrid Load feed by AC Grid.

A. *Normal operations:*

Figs. (8-10) illustrate dynamic simulation responses of Power, Power Factor, Reactive Power, RMS Voltage at Load bus in presence of HSCC FACTS controlled by HFLC and PID controllers and without HSCC FACTS under normal operation conditions.

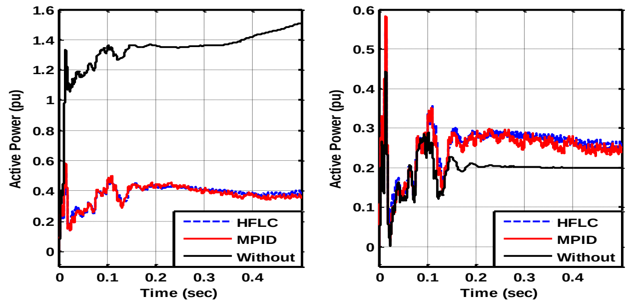

Fig 8: Active Power at Generator and Load Buses.

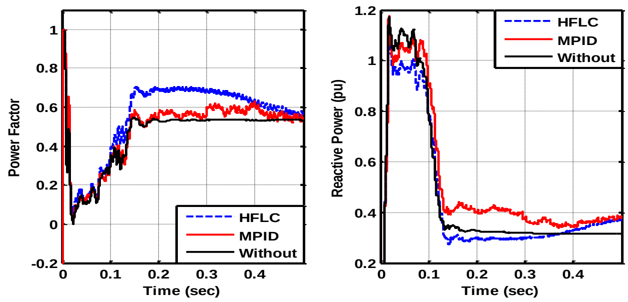

Fig 9: Power Factor and Reactive power at Load Bus.

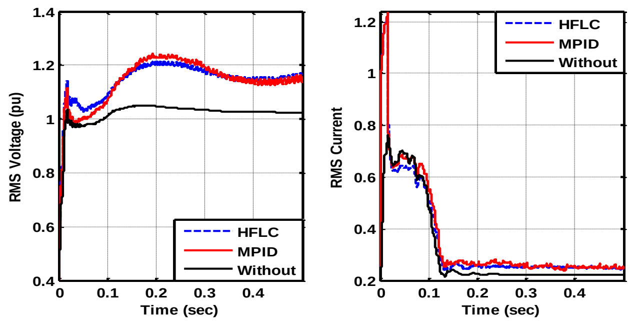

Fig 10: RMS Voltage and RMS current at Load Buses.

B. *Load Excursions*

The AC system is examined under load excursion as the following:

Linear load rejected at time = 0.1-0.15 sec, Non-Linear load rejected at time = 0.2- 0.25 sec, Motor load Torque; Tm at =50 % at time = 0.3-0.35 sec and Motor load Torque; Tm at =150% at time = 0.4-0.45 sec. Figs. (11-13) illustrate simulation responses of Power, Power Factor, Reactive Power, RMS-Voltage at Load bus in presence of HSCC FACTS controlled by HFLC and PID controllers and without HSCC FACTS.

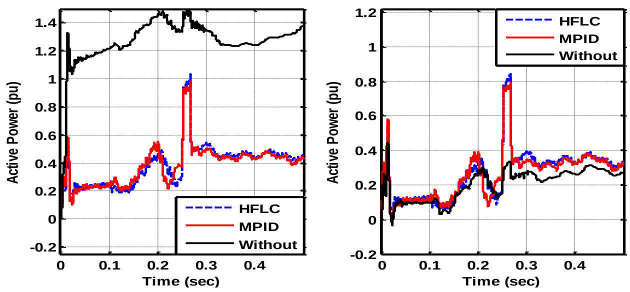

Fig 11: Active Power at Generator and Load Buses.

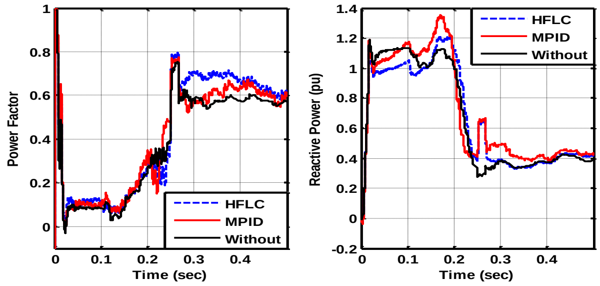

Fig 12: Power Factor and Reactive power at Load Bus.

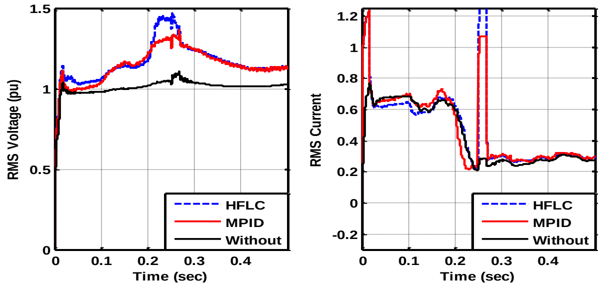

Fig 13: RMS Voltage and RMS current at Load Buses.

C. Short Circuit Faults

The AC system is examined under short circuit fault for time = 0.2-0.3 at Vs bus. Figs. (14-16) illustrate simulation responses of Power, Power Factor, Reactive Power, RMS-Voltage at Load bus in presence of HSCC FACTS controlled by HFLC and PID controllers and without HSCC FACTS.

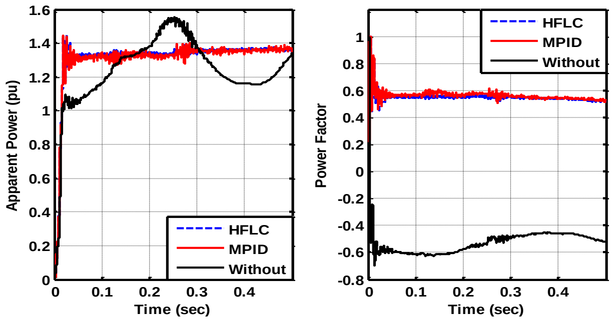

Fig 14: Active Power at Generator and Load Buses.

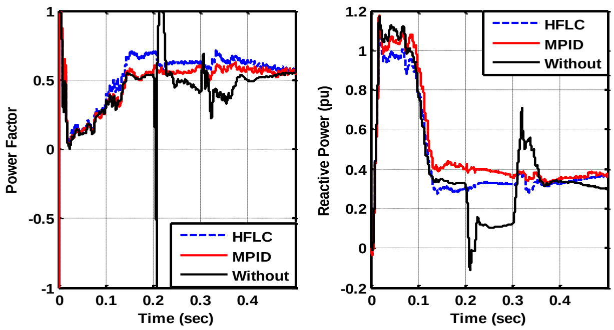

Fig 15: Power Factor and Reactive power at Load Bus.

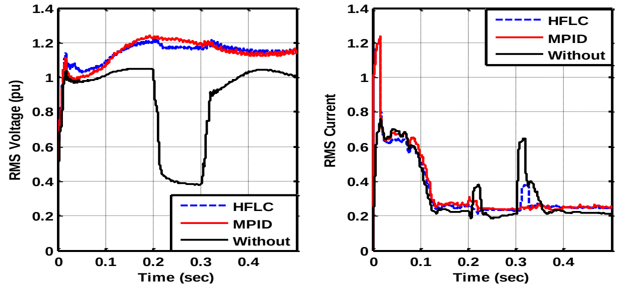

Fig 16: RMS Voltage and RMS current at Load Buses.

D. Open Circuit Faults

The AC system is examined under open circuit fault for time = 0.2-0.3 at Vs bus. Figs. (17-19) illustrate simulation responses of Power, Power Factor, Reactive Power, RMS Voltage at Load bus in presence of HSCC FACTS controlled by HFLC and PID controllers and without HSCC FACTS.

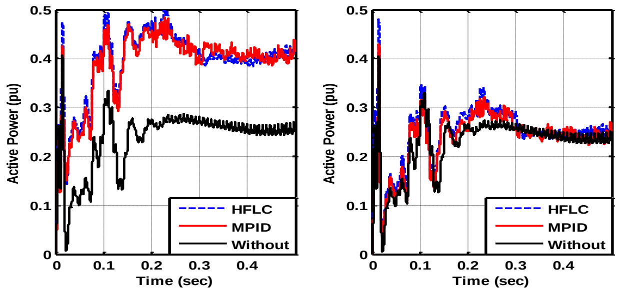

Fig 17: Active Power at Generator and Load Buses.

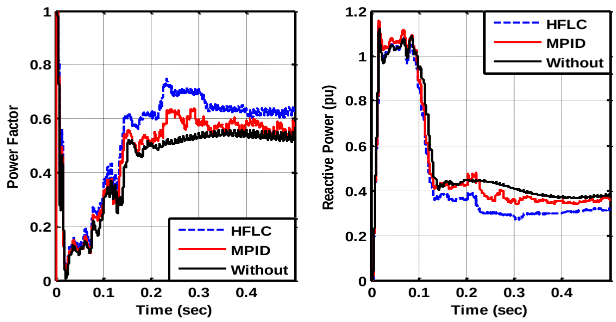

Fig 18: Power Factor and Reactive power at Load Bus.

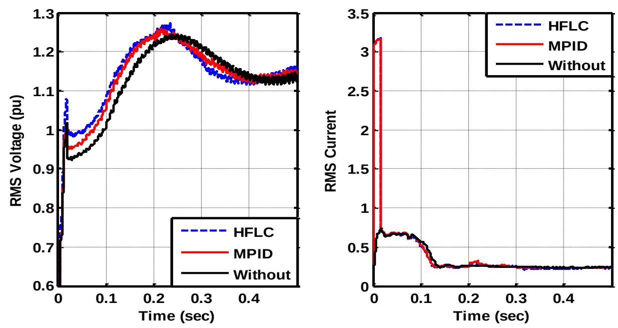

Fig 19: RMS Voltage and RMS current at Load Buses.

VI. CONCLUSION

The paper presents a hybrid FACTS Based Voltage stabilization and Loss reduction soft starting scheme for smart Grid Dynamic Inrush and Nonlinear Loads. The

Two-Stage Hierarchical Fuzzy Logic Control Scheme is based on a tri-loop error design is investigated for test system. HFLC is utilized to reduce the number of fuzzy rules to a linear function of input variables. Designing an HFLC consists of dividing a global task into sub-levels, designing an independent FLC for each sub-level, and, devising a strategy for coordinating the sub-controllers to achieve the global objective. The simulation results validate the proposed control scheme effectiveness and robustness with Efficient Energy Utilization, improved power quality and Power Factor at the Common AC Bus and load bus. The same scheme is now tested for Dynamic Voltage Regulation and Loss reduction in Smart grid distribution and Utilization grid Systems.

APPENDIX

Steam Turbine:	Pout=600MW, Speed=3600 rpm.		
Synchronous Generator:	*3Ph.*, 2 poles		
	Vg=25 KV (L-L), Sg= 600MVA		
	Xd=1.79 pu	Xd'=0.169 pu	Xd"=0.135 pu
	Xq=1.71 pu	Xq'=0.228 pu	Xq"=0.2 pu
	X1=0.13 pu		
Transmission line:	500 KV (L-L), 300km		
	R/km=0.01273Ω, L/km=0.9337mH		
Infinite Bus:	500KV		
HSCC Parameters:	$C_{f1}= C_{f2}=250\ \mu f$ $C_L=15\ \mu f$, $R_f=1.5\Omega$, $L_f=3\ mH$		
SPWM:	$P_2= P_3= \overline{P_1}$, Fs/w = 1750 Hz		

HFLC linguistic variables : *mf: membership function.* *NL; Negative Large.* *NS; Negative Small.* *Z; Zero.* *PS; Positive Small.* *PL; Large.*		***Tri-Loop:*** T_1=5 ms T_2=10 ms T_3=5 ms T_4=20 ms T_5=30 ms T_6=20 ms Delay=5-10 ms $\gamma_{Vg}=1$ $\gamma_{Pg}=0.25$ $\gamma_{Ig}=0.5$ $\gamma_{Vg\_rep}=1$ $\gamma_{Pg\_rep}=1$ $\gamma_{Ig\_rep}=0.5$ Kc=1 **Controller gains:** Kp=0-15 , Ki=0-1; Kd=0-1, Ke=0-1
PDFLC	**PIDFLC**	
Input variables: global error (e_t) and change of error ($\acute{e}_t$). **Output variable:** PD value.	**Input variables:** PD value and the error integrator $\int e_t$. **Output variable:** The output signal (U)	

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